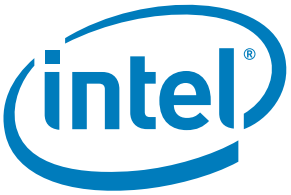

PCI Express* (PCIe*) 4.0 Retimer Supplemental Features and Standard BGA Footprint

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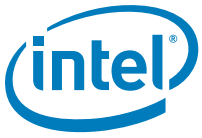
Revision 004

June 2018

Document Number: 336467-004US



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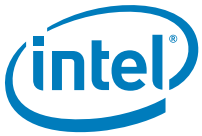


Revision History

Document Number	Revision Number	Description	Date
336467	001	• Initial Release	November 2017
336467	002	• Updated the register configuration section to define 32-bit registers instead of 8-bit registers. • Updated proposed register offset map to include vendor defined registers, reserved registers, and 16-bit addressing. • Added SMBus Command Code definition and examples. • Made REFCLK_OUT a required feature. • Changed names for the SMB_ADDR pins from (0,1,2) to (1,2,3). • Updated the specification reference list to include the *PCIe* Base Specification* Rev 4.0, Ver 1.0. • Updated support for EEPROM configuration load to Optional. • Added Link Subdivision details. • Added frequency requirements for SMBus implementation.	February 2018
336467	003	• Correct PCI Express naming.	March 2018
336467	004	• X16 Retimer Interface signals, changed pin FJ3 description to “data” • X16 Retimer Interface signals, changed pin FF5 description to “clock” • X8 Retimer Interface signals, changed pin AP11 to “EE_CLK” • X8 Retimer Interface signals, changed pin AP13 to “EE_DAT” • X8 Retimer Interface signals, removed VD_12 signal from miscellaneous section • X8 Retimer Interface signals, Receiver differential pair, B channel, Lane 3, “p” pin changed to “U2” • X8 Retimer Interface signals, corrected signal name to “SMB_ADDR_3/VD_12” • X4 Retimer Interface signals, changed pin U8 description to “data”, • X4 Retimer Interface signals, changed pin N8 description to “clock” • X4 Retimer Interface signals, updated pin A5 to VD_5 • X4 Retimer Interface signals, updated pin U8 to EE_DAT/VD_7 • X4 Retimer Interface signals, updated pin N8 to EE_CLK/VD_8 • X4 Retimer Interface signals, updated pin C8 to VD_9 • X4 Retimer Interface signals, updated pin W9 to SMB_ADDR_3/VD_10 • X4 Retimer Interface signals, updated pin A10 to VD_6 • Renamed a few sections between 3.2 and 3.15 to maintain naming consistency	June 2018

§

1 Introduction

1.1 Overview

PCI Express* (PCIe*) 4.0 capable retimers extend the channel reach on a platform to beyond what is possible otherwise.

With PCI Express 4.0 (16 GT/s), data rate has increased by 2x compared to previous generation (8 GT/s), resulting in shorter channel reach. Common use cases include channels expanding over system boards, backplanes, cables, risers, and add-in cards. Such long channels can have loss that far exceeds the spec loss target of -28 dB at 8 GHz. Retimer is now part of the *PCI Express 4.0 Base Specification*. PCI-SIG* is expected to implement compliance program for testing retimers.

It is expected that significant number of platforms using PCI Express 4.0 will require retimers. Multiple sources of retimers will make adoption of PCIe 4.0 technology easier. Common footprint simplifies the platform design process. Pinout is optimized for 16 GT/s signal integrity and thermal challenges.

Figure 1-1 to Figure 1-4 show few example configurations involving riser, mother board and add-in card. Various other configurations are possible.

Figure 1-1. Platform Configuration with an Add-in Card and Retimer on Mother Board

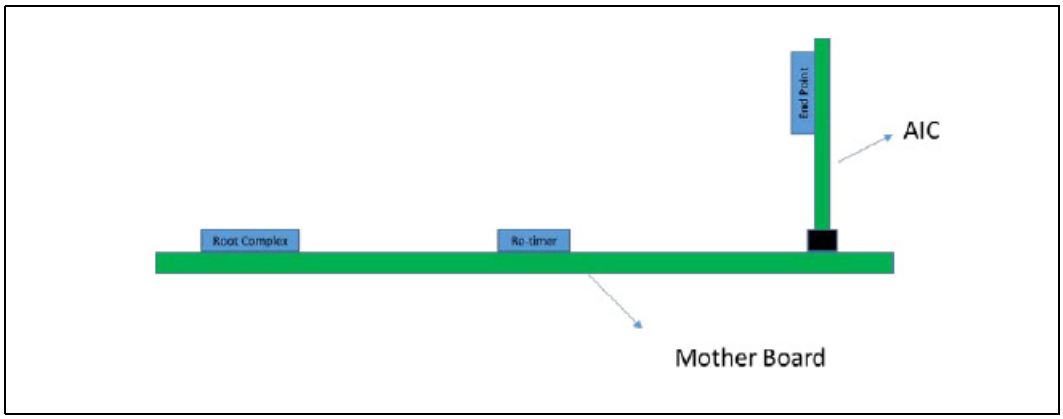


Figure 1-2. Platform Configuration with an Add-in Card and Riser, Retimer on Riser

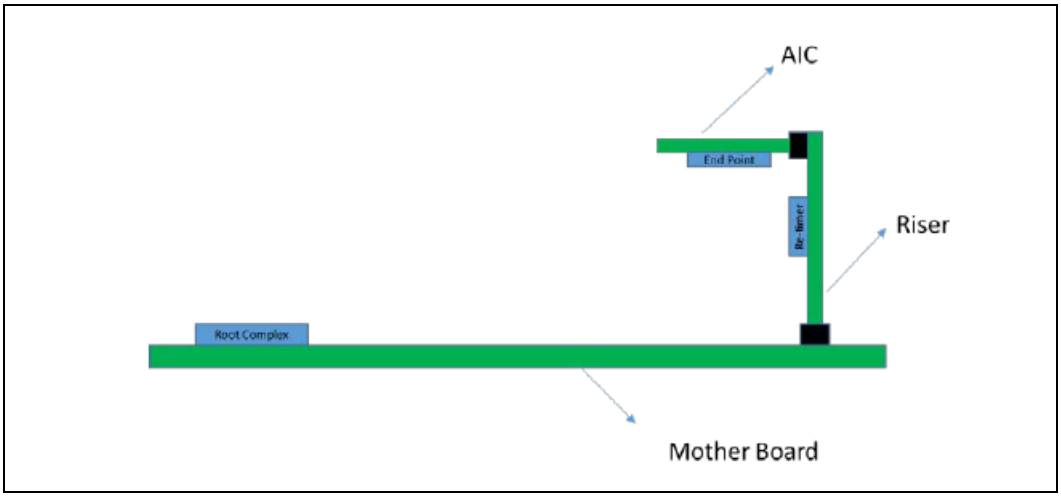


Figure 1-3. Platform Configuration with a Riser and Cable, Retimer is on Riser

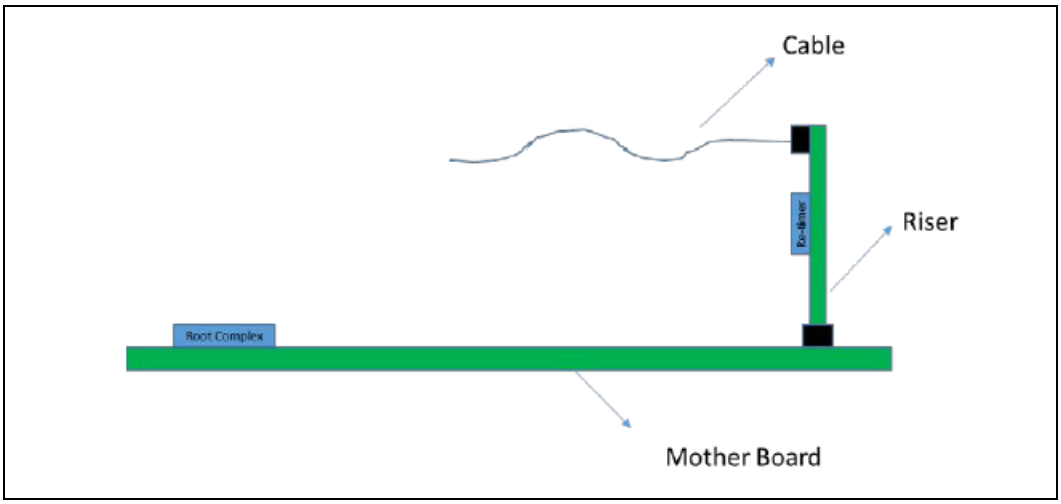
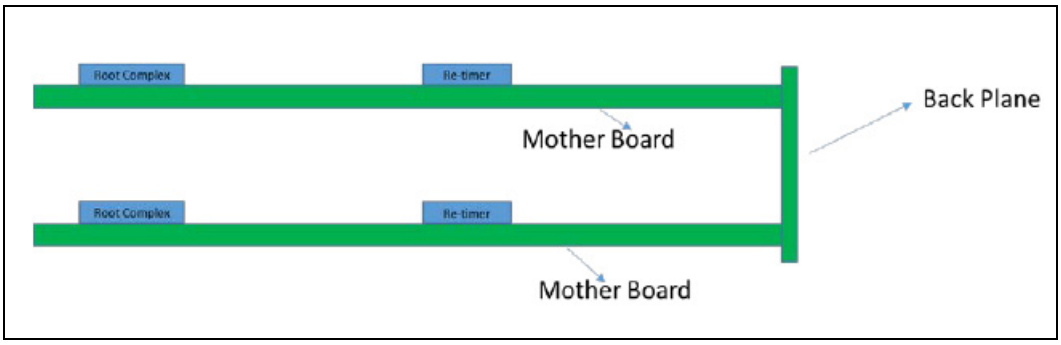


Figure 1-4. Platform Configuration with a Backplane, Retimer on Both Mother Boards



1.2 Terminology

The "#" symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when the signal is at a high voltage level.

The following notations are used to describe the various signal types.

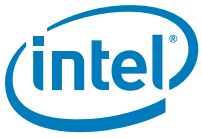
Table 1-1. Abbreviations

Term	Description
I	Input
O	Output
I/O	Bi-Directional
PU	Pull-up
PWR	Power
GND	Ground
Host	This term is synonymous with platform or system
NC	No Connect
VD	Vendor Defined
SSC	Spread Spectrum Clocking
SRIS	Separate Reference Clock Independent SSC
RX	PCIe Receiver
TX	PCIe Transmitter
N/A	Not Applicable

1.3 Specification References

This specification requires references to other specifications or documents that will form the basis for some of the requirements stated herein.

- *PCI Express Card Electromechanical (CEM) Specification*, Revision 4.0, Version 0.5, December 18, 2015
- *PCI Express Base Specification*, Revision 4.0, Version 1.0, October 5, 2017
- *System Management Bus (SMBus) Specification*, Version 2.0, August 3, 2000
- *JTAG Specification* (IEEE* 1149.1)
- *I^2C* BUS Specifications*, Version 2.1, January 2000



1.4 Retimer Supplemental Features Beyond PCIe 4.0 Specification

Table 1-2. Retimer Feature Comparison

Feature	*PCIe 4.0 Base Specification for Retimers*	*PCIe 4.0 for Retimers Supplemental Features and Standard BGA Footprint Specification*
SRIS	Optional	Required
Slave Loopback	Optional	Required
Receiver Lane Margining (Voltage)	Optional	Required
Link Subdivision(1) (Bifurcation)	Not defined explicitly but can be supported	Required
L1PM Substates(2)	Optional	Required
SMBus Programmable Configurations	N/A	Required
Support for EEPROM load configuration	N/A	Optional
Retimer Common (size, pinout) Footprint	N/A	Required
Reference Clock Out	N/A	Required

Notes:
1. Link subdivision should be implemented such that no power reset is required.
2. L1PM Substate support for retimers as defined in Section 4.3.10 in the *PCIe Base Specification*.

1.4.1 Link Subdivision

Link Subdivision (also known as bifurcation) is dividing a PCIe Link into a certain number of independent links. Each of the sub divided links behave as an independent PCIe link and is required is follow the PCIe Link requirements. For example, each of these subdivided links should support defaulting to x1 Link width if the link cannot be trained at the required link width.

The host updates the Global Parameter register in the retimer with required link subdivision using SMBus commands. Refer to Section 6.2 and Section 6.4.

A host is required to issue a warm reset to the retimer to retrain the link with updated link subdivision settings.

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2 Mechanical Specification

2.1 Overview

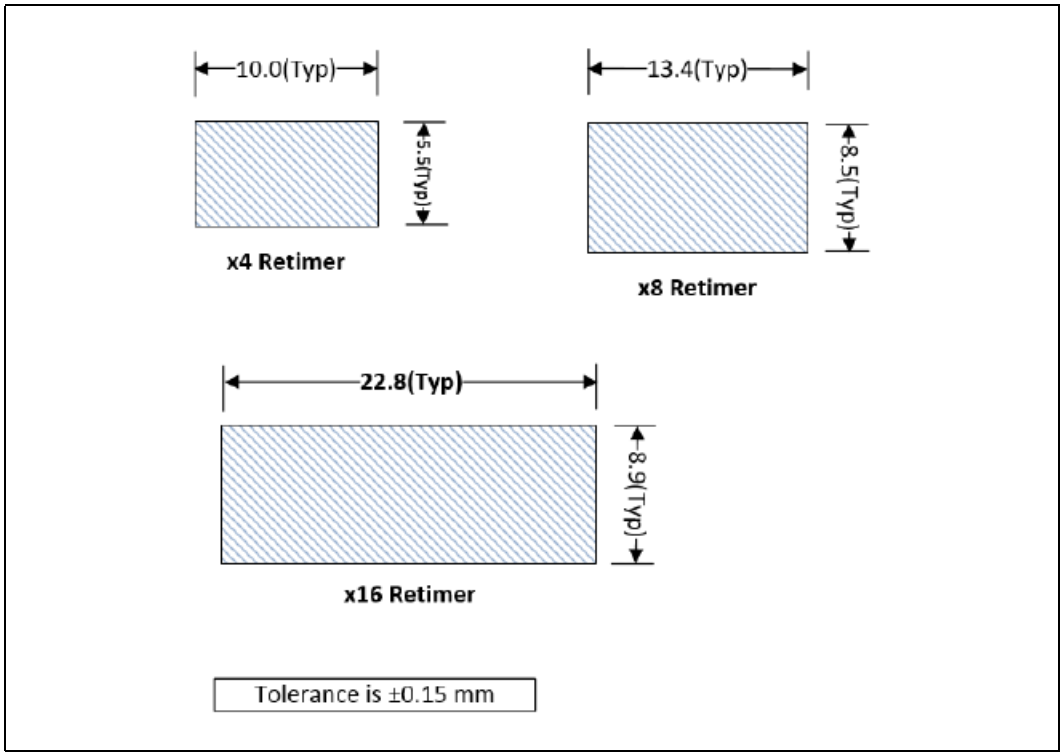
Three different retimer package sizes are specified.

- x4: Supports 4 lanes in upstream direction and 4 lanes in downstream direction
- x8: Supports 8 lanes in upstream direction and 8 lanes in downstream direction
- x16: Supports 16 lanes in upstream direction and 16 lanes in downstream direction

The following figure shows the overall package dimensions for the three retimer form factors.

Note: All the dimensions are in mm and the tolerance is ±0.15 mm.

Figure 2-1. Retimer Form Factors



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3 Signal Description

This chapter provides a detailed description of retimer signals. The signal descriptions are arranged in functional groups according to their associated interface.

Signal directions in Table 3-1, "x16 Retimer Signal Descriptions", Table 3-2, "x8 Retimer Signal Descriptions" and Table 3-3, "x4 Retimer Signal Descriptions" are from retimer perspective. That is, "O" indicates output from the retimer device and "I" indicates input to the retimer device.

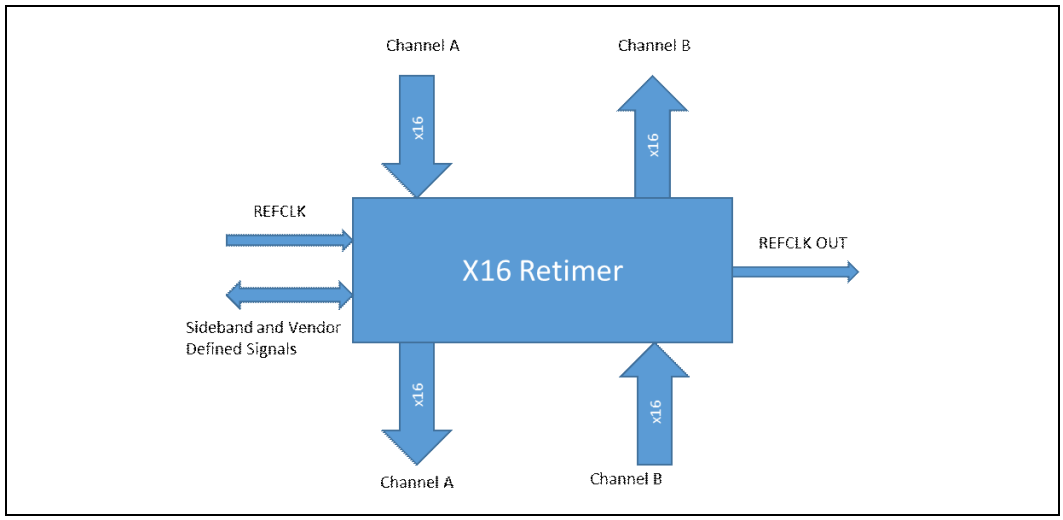
Signals labeled "VD" are Vendor Defined. It is required that VD balls carry signals that are not critical to retimer basic functionality and are used for providing enhanced or debug features.

Common footprint for following link widths are defined for the PCIe 16 GT/s retimers:

1. x16 (link with 16 physical lanes)
2. x8 (link with 8 physical lanes)
3. x4 (link with 4 physical lanes)

The following figure shows the x16 retimer block diagram. Channel A and Channel B are ports that can be configured to be upstream or downstream.

Figure 3-1. x16 Retimer Block Diagram



3.1 x16 Retimer Interface Signals

The following table lists pin numbers and functions for each of the pins in the x16 pinout, along with voltage level wherever applicable.

Table 3-1. x16 Retimer Signal Descriptions (Sheet 1 of 5)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/O				
M26	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
P29	A_PETn0	O		
W26	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
AA29	A_PETn1	O		
AF26	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
AH29	A_PETn2	O		
AN26	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
AR29	A_PETn3	O		
AY26	A_PETp4	O	Transmitter differential pair, A Channels, Lane 4	
BB29	A_PETn4	O		
BG26	A_PETp5	O	Transmitter differential pair, A Channels, Lane 5	
BJ29	A_PETn5	O		
BP26	A_PETp6	O	Transmitter differential pair, A Channels, Lane 6	
BT29	A_PETn6	O		
CA26	A_PETp7	O	Transmitter differential pair, A Channels, Lane 7	
CC29	A_PETn7	O		
CH26	A_PETp8	O	Transmitter differential pair, A Channels, Lane 8	
CK29	A_PETn8	O		
CR26	A_PETp9	O	Transmitter differential pair, A Channels, Lane 9	
CU29	A_PETn9	O		
DB26	A_PETp10	O	Transmitter differential pair, A Channels, Lane 10	
DD29	A_PETn10	O		
DJ26	A_PETp11	O	Transmitter differential pair, A Channels, Lane 11	
DL29	A_PETn11	O		
DT26	A_PETp12	O	Transmitter differential pair, A Channels, Lane 12	
DV29	A_PETn12	O		
EC26	A_PETp13	O	Transmitter differential pair, A Channels, Lane 13	
EE29	A_PETn13	O		
EK26	A_PETp14	O	Transmitter differential pair, A Channels, Lane 14	
EM29	A_PETn14	O		
EU26	A_PETp15	O	Transmitter differential pair, A Channels, Lane 15	
EW29	A_PETn15	O		
N34	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
R35	B_PERn0	I		
Y34	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
AB35	B_PERn1	I		

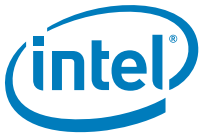


Table 3-1. x16 Retimer Signal Descriptions (Sheet 2 of 5)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
AG34	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
AJ35	B_PERn2	I		
AP34	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
AT35	B_PERn3	I		
BA34	B_PERp4	I	Receiver differential pair, B Channels, Lane 4	
BC35	B_PERn4	I		
BH34	B_PERp5	I	Receiver differential pair, B Channels, Lane 5	
BK35	B_PERn5	I		
BR34	B_PERp6	I	Receiver differential pair, B Channels, Lane 6	
BU35	B_PERn6	I		
CB34	B_PERp7	I	Receiver differential pair, B Channels, Lane 7	
CD35	B_PERn7	I		
CJ34	B_PERp8	I	Receiver differential pair, B Channels, Lane 8	
CL35	B_PERn8	I		
CT34	B_PERp9	I	Receiver differential pair, B Channels, Lane 9	
CV35	B_PERn9	I		
DC34	B_PERp10	I	Receiver differential pair, B Channels, Lane 10	
DE35	B_PERn10	I		
DK34	B_PERp11	I	Receiver differential pair, B Channels, Lane 11	
DM35	B_PERn11	I		
DU34	B_PERp12	I	Receiver differential pair, B Channels, Lane 12	
DW35	B_PERn12	I		
ED34	B_PERp13	I	Receiver differential pair, B Channels, Lane 13	
EF35	B_PERn13	I		
EL34	B_PERp14	I	Receiver differential pair, B Channels, Lane 14	
EN35	B_PERn14	I		
EV34	B_PERp15	I	Receiver differential pair, B Channels, Lane 15	
EY35	B_PERn15	I		
R1	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
N2	A_PERn0	I		
AB1	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
Y2	A_PERn1	I		
AJ1	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
AG2	A_PERn2	I		
AT1	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
AP2	A_PERn3	I		
BC1	A_PERp4	I	Receiver differential pair, A Channels, Lane 4	
BA2	A_PERn4	I		
BK1	A_PERp5	I	Receiver differential pair, A Channels, Lane 5	
BH2	A_PERn5	I		

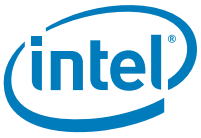


Table 3-1. x16 Retimer Signal Descriptions (Sheet 3 of 5)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
BU1	A_PERp6	I	Receiver differential pair, A Channels, Lane 6	
BR2	A_PERn6	I		
CD1	A_PERp7	I	Receiver differential pair, A Channels, Lane 7	
CB2	A_PERn7	I		
CL1	A_PERp8	I	Receiver differential pair, A Channels, Lane 8	
CJ2	A_PERn8	I		
CV1	A_PERp9	I	Receiver differential pair, A Channels, Lane 9	
CT2	A_PERn9	I		
DE1	A_PERp10	I	Receiver differential pair, A Channels, Lane 10	
DC2	A_PERn10	I		
DM1	A_PERp11	I	Receiver differential pair, A Channels, Lane 11	
DK2	A_PERn11	I		
DW1	A_PERp12	I	Receiver differential pair, A Channels, Lane 12	
DU12	A_PERn12	I		
EF1	A_PERp13	I	Receiver differential pair, A Channels, Lane 13	
ED2	A_PERn13	I		
EN1	A_PERp14	I	Receiver differential pair, A Channels, Lane 14	
EL2	A_PERn14	I		
EY1	A_PERp15	I	Receiver differential pair, A Channels, Lane 15	
EV2	A_PERn15	I		
M7	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
P10	B_PETn0	O		
W7	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
AA10	B_PETn1	O		
AF7	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
AH10	B_PETn2	O		
AN7	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
AR10	B_PETn3	O		
AY7	B_PETp4	O	Transmitter differential pair, B Channels, Lane 4	
BB10	B_PETn4	O		
BG7	B_PETp5	O	Transmitter differential pair, B Channels, Lane 5	
BJ10	B_PETn5	O		
BP7	B_PETp6	O	Transmitter differential pair, B Channels, Lane 6	
BT10	B_PETn6	O		
CA7	B_PETp7	O	Transmitter differential pair, B Channels, Lane 7	
CC10	B_PETn7	O		
CH7	B_PETp8	O	Transmitter differential pair, B Channels, Lane 8	
CK10	B_PETn8	O		
CR7	B_PETp9	O	Transmitter differential pair, B Channels, Lane 9	
CU10	B_PETn9	O		

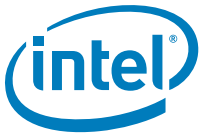


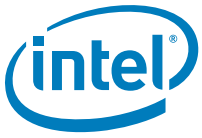
Table 3-1. x16 Retimer Signal Descriptions (Sheet 4 of 5)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
DB7	B_PETp10	O	Transmitter differential pair, B Channels, Lane 10	
DD10	B_PETn10	O		
DJ7	B_PETp11	O	Transmitter differential pair, B Channels, Lane 11	
DL10	B_PETn11	O		
DT7	B_PETp12	O	Transmitter differential pair, B Channels, Lane 12	
DV10	B_PETn12	O		
EC7	B_PETp13	O	Transmitter differential pair, B Channels, Lane 13	
EE10	B_PETn13	O		
EK7	B_PETp14	O	Transmitter differential pair, B Channels, Lane 14	
EM10	B_PETn14	O		
EU7	B_PETp15	O	Transmitter differential pair, B Channels, Lane 15	
EW10	B_PETn15	O		
Reference Clock				
FJ16	REFCLK+	I	100 MHz. Reference Clock (Differential Pair) to be used in Common Clock configuration, as defined by the *PCIe Base Specification*	
FF18	REFCLK-	I		
B16	REFCLK_Out+ (2)	O	100 MHz. This pin is used for driving REFCLK_out+	
E18	REFCLK_Out1 (2)	O	100 MHz. This pin is used for driving REFCLK_out -	
PCI Express Auxiliary Signals				
F2	PERST#	I	Fundamental Reset; Active Low	1.8V (3.3V tolerant)
G35	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8V (3.3V tolerant)
JTAG				
B6	JTAG_TDI	I	JTAG Test Data In	1.8V (3.3V tolerant)
B9	JATG_TDO	O	JTAG Test Data Out; Open drain; Require pull up on the platform; Pull up voltage must be selected based on the I/O voltage selected for other JTAG signals	
B12	JTAG_TMS	I	JTAG Test Mode Select	1.8V (3.3V tolerant)
B3	JTAG_TCK	I	JTAG Clock	1.8V (3.3V tolerant)
E8	JTAG_TRST#	I	JTAG Reset; Active Low	1.8V (3.3V tolerant)

Table 3-1. x16 Retimer Signal Descriptions (Sheet 5 of 5)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
System Management Bus (SMBus)				
B31	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8V (3.3V tolerant)
B28	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8V (3.3V tolerant)
F34	SMB_ADDR_1	I	SMBus Address Bit1	1.8V (3.3V tolerant)
B23	SMB_ADDR_2	I	SMBus Address Bit2	1.8V (3.3V tolerant)
B25	SMB_ADDR_3/ VD_16(1)	I	SMBus Address Bit3 or Vendor Defined	1.8V (3.3V tolerant)
EEPROM Configuration Interface				
FJ3	EE_DAT/VD_7(1)	I/O	EEPROM Interface Data or Vendor Defined	1.8V (3.3V tolerant)
FF5	EE_CLK/VD_8(1)	I/O	EEPROM Interface Clock or Vendor Defined	1.8V (3.3V tolerant)
Miscellaneous				
FJ23	VD_1(1)	TBD	Vendor Defined Signal	
FF24	VD_2(1)	TBD	Vendor Defined Signal	
FJ6	VD_3(1)	TBD	Vendor Defined Signal	
FF8	VD_4(1)	TBD	Vendor Defined Signal	
FJ9	VD_5(1)	TBD	Vendor Defined Signal	
FF11	VD_6(1)	TBD	Vendor Defined Signal	
FJ25	VD_9(1)	TBD	Vendor Defined Signal	
FF27	VD_10(1)	TBD	Vendor Defined Signal	
FJ28	VD_11(1)	TBD	Vendor Defined Signal	
FF30	VD_12(1)	TBD	Vendor Defined Signal	
FJ31	VD_13(1)	TBD	Vendor Defined Signal	
FF33	VD_14(1)	TBD	Vendor Defined Signal	
G1	VD_15(1)	TBD	Vendor Defined Signal	
E11	RX_DET_BYP	I	Receiver Detection Bypass	
Power				
6 pins	PWR_1	Power Rail 1	1.8V or 3.3V	
24 pins	PWR_2	Power Rail 2	1.1V or 1.0V or 0.9V or 0.8V	
152pins	GND		0V	

Notes:
1. It is safe to route high speed Vendor Defined (VD) signals at these locations. Care must be taken to provide enough GND isolation. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins.
2. REFCLK Out is compliant with REFCLK definition in the *PCIe Base Specification*.



3.1.1 Signal Descriptions

3.1.1.1 SMBus Interface

SMBCLK, SMBDAT and three address pins (SMB_ADDR_1, SMB_ADDR_2, SMB_ADDR_3) are assigned in the ballmap. Three address bits are required to address retimers on the SMBus in a platform configuration. Retimer vendors are allowed to take care of SMBus address needs on the platform by using only two address pins, if they can take care of additional addresses needed by the platform in a proprietary way. The retimer vendors can use the third address bit for Vendor Defined purposes in that case.

Address pin SMB_ADDR_3 can be used for Vendor Defined signal.

SMBus implementation is required to support 100 kHz and be 400 kHz compatible.

3.1.1.2 EEPROM Interface

EECLK and EEDAT signals are defined to load initial configuration from an external EEPROM. No specific interface is mentioned, giving retimer vendors freedom to use the interface of their choice. An example of the interface that can be used is I^2C.

When this dedicated interface is not used for EEPROM load, and some other means are used to load EEPROM configuration, these pin can be used as Vendor Defined.

3.1.1.3 Miscellaneous Signals

3.1.1.3.1 RX_DET_BYP (PCIe_BYPASS_MODE)

This signal is asserted to bypass the receiver detection process to expedite the link training. In this mode, the retimer does not do any active determination of its receiver impedance. It rather assumes that the receiver is present on the other end of the link. This feature can be used for soldered-down devices. The same signal when asserted, also serves to bypass the PCIe mode.

3.1.1.3.2 REFCLK_Out+/REFCLK_Out-

This is the 100 MHz reference clock as defined by the *PCIe Base Specification*. Retimer devices are required to provide this clock output to ease clock routing complexities on the platform.

3.1.1.3.3 PERST#

Fundamental Reset signal as defined by the *PCIe Base Specification*.

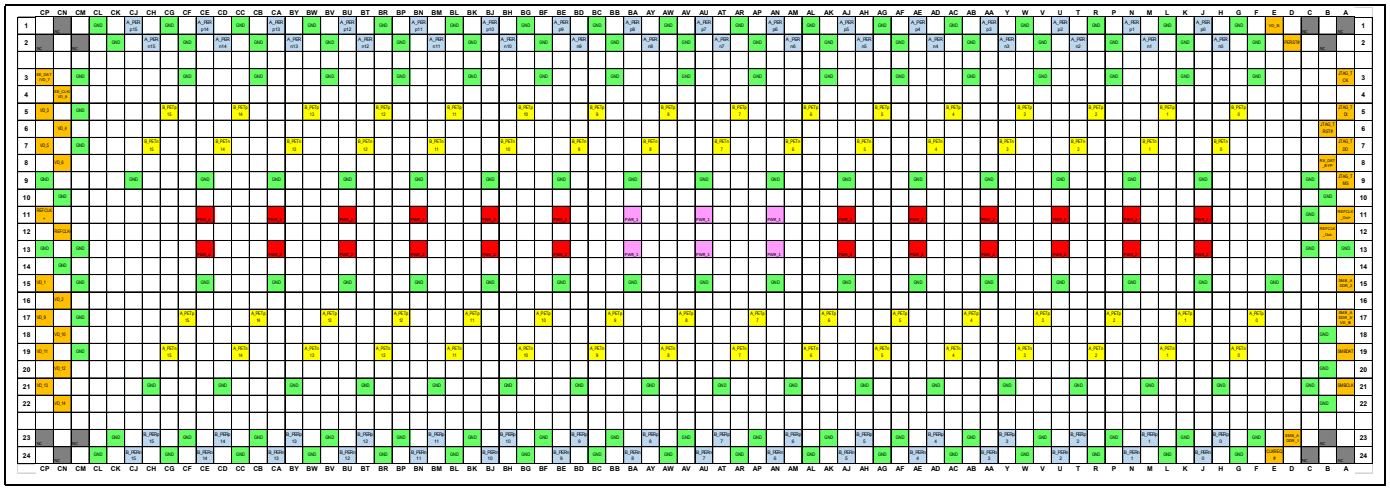
3.1.1.3.4 CLKREQ#

This signal is used to support L1PM Substates. Refer to the PCIe Base Specification for more details on L1PM Substate support for retimers.

3.2 x16 Retimer Ballmap (Package Side)

The following figure shows the ball arrangement from the retimer package side. Note that this figure is for reference only, for actual pin number and spacing details, refer to Figure 3-5, "x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)" on page 21.

Figure 3-2. x16 Retimer, Package Side Pin Arrangement (Top View)



Note: Refer to Figure 3-5, "x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)" on page 21 for pitch and spacing details.

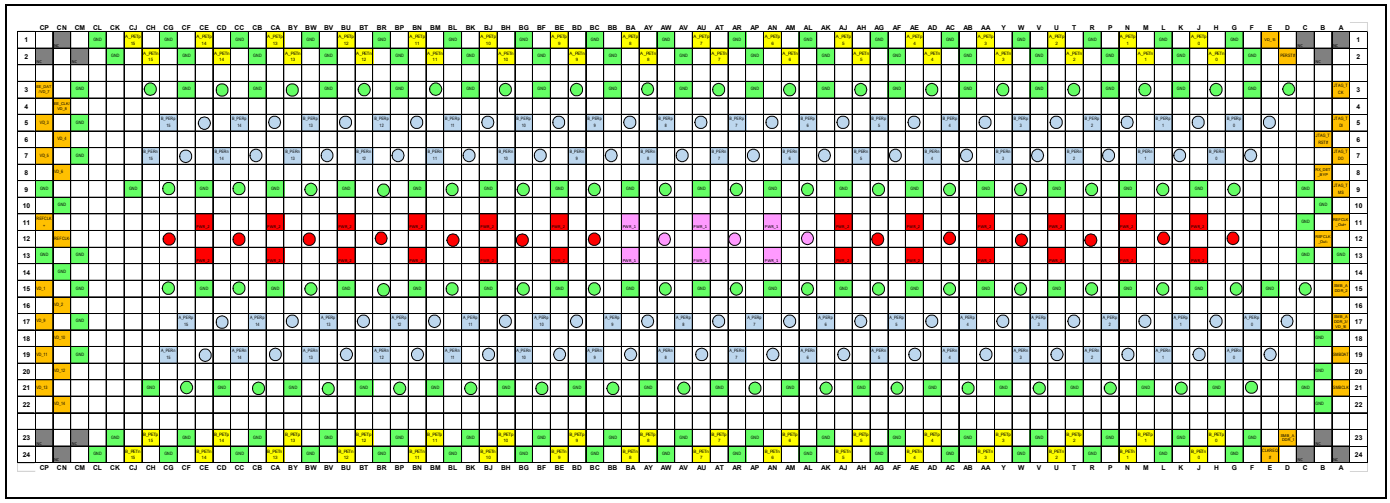
Legend	
	PWR_1
	PWR_2
	GND
	Control and VD Signals
	Differential TX
	Differential RX
	No Balls
	NC

3.3 x16 Retimer Ballmap (Platform Side)

The following figure shows the platform side pin arrangement with PCB vias. The TX and RX balls here have been swapped when compared to package side ballmap (Figure 3-2). That is, “TX lane x” in package side ballmap gets mapped to “RX lane x” in the land pattern.

Note that this figure is for reference only; for actual pin number and spacing details, refer to Figure 3-5, “x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)” on page 21.

Figure 3-3. x16 Retimer, Platform side Pin Arrangement (Top View)

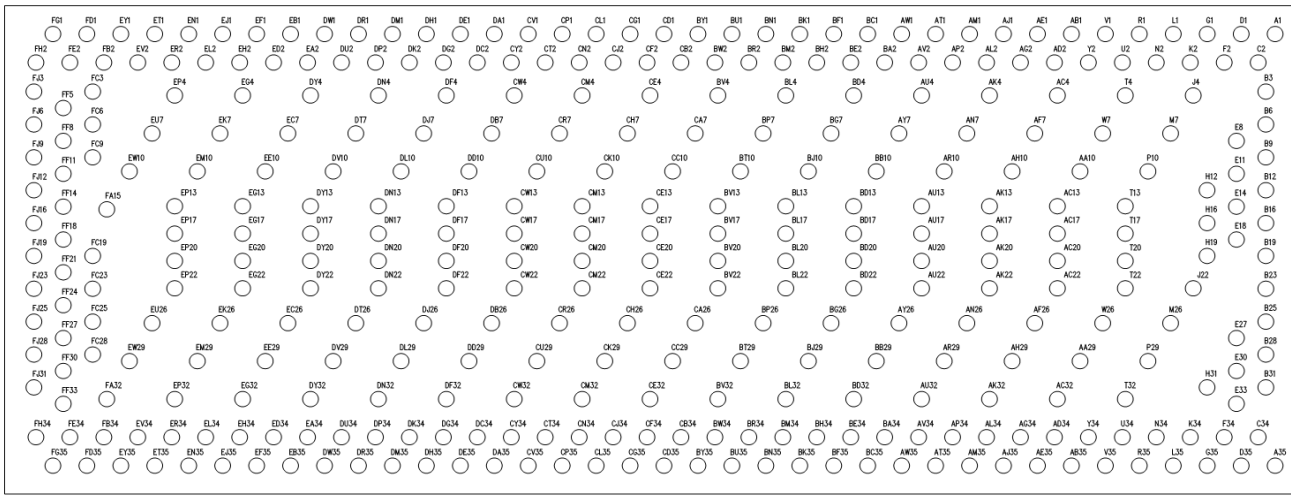


Legend	
	RX Via
	PWR_1 Via
	PWR_2 Via
	GND Via
	Control Signal Via

3.4 x16 Retimer, Physical Ballmap (Package Side)

The following figure shows the top view of x16 retimer package-side ball arrangement with pin numbers.

Figure 3-4. x16 Retimer, Physical Ballmap on Package (Top View)

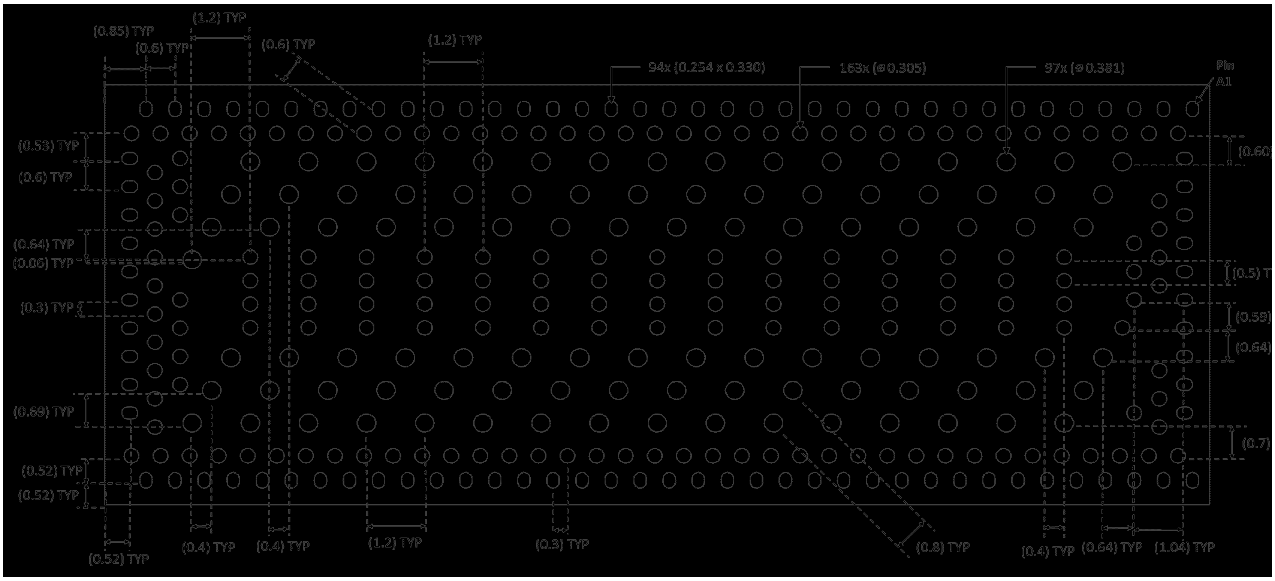


3.5 x16 Retimer Platform Side Land Pattern

The following figure shows top view of the platform side mechanical outline drawing for x16 retimer.

Dimension tolerances for ball diameter are ±0.05 mm.

Figure 3-5. x16 Retimer, Platform Side Land Pattern with Spacing Details (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.6 x8 Retimer Interface Signals

Table 3-2. x8 Retimer Signal Descriptions (Sheet 1 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/Os				
B9	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
A10	A_PETn0	O		
C6	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
D7	A_PETn1	O		
B3	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
A4	A_PETn2	O		
E2	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
D1	A_PETn3	O		
AB1	A_PETp4	O	Transmitter differential pair, A Channels, Lane 4	
AA2	A_PETn4	O		

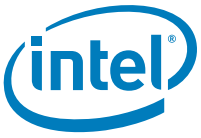


Table 3-2. x8 Retimer Signal Descriptions (Sheet 2 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
AE4	A_PETp5	O	Transmitter differential pair, A Channels, Lane 5	
AD3	A_PETn5	O		
AH1	A_PETp6	O	Transmitter differential pair, A Channels, Lane 6	
AG2	A_PETn6	O		
AL4	A_PETp7	O	Transmitter differential pair, A Channels, Lane 7	
AK3	A_PETn7	O		
B15	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
A14	A_PERn0	I		
C18	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
D17	A_PERn1	I		
B21	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
A20	A_PERn2	I		
E22	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
D23	A_PERn3	I		
AB23	A_PERp4	I	Receiver differential pair, A Channels, Lane 4	
AA22	A_PERn4	I		
AE20	A_PERp5	I	Receiver differential pair, A Channels, Lane 5	
AD21	A_PERn5	I		
AH23	A_PERp6	I	Receiver differential pair, A Channels, Lane 6	
AG22	A_PERn6	I		
AL20	A_PERp7	I	Receiver differential pair, A Channels, Lane 7	
AK21	A_PERn7	I		
H21	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
G20	B_PETn0	O		
L22	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
K23	B_PETn1	O		
P21	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
N20	B_PETn2	O		
U22	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
T23	B_PETn3	O		
AP23	B_PETp4	O	Transmitter differential pair, B Channels, Lane 4	
AN22	B_PETn4	O		
AU20	B_PETp5	O	Transmitter differential pair B Channels, Lane 5	
AT21	B_PETn5	O		
AP17	B_PETp6	O	Transmitter differential pair, B Channels, Lane 6	
AR18	B_PETn6	O		
AU14	B_PETp7	O	Transmitter differential pair, B Channels, Lane 7	
AT15	B_PETn7	O		
H3	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
G4	B_PERn0	I		

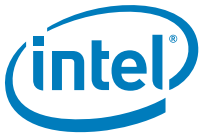


Table 3-2. x8 Retimer Signal Descriptions (Sheet 3 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
L2	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
K1	B_PERn1	I		
P3	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
N4	B_PERn2	I		
U2	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
T1	B_PERn3	I		
AP1	B_PERp4	I	Receiver differential pair, B Channels, Lane 4	
AN2	B_PERn4	I		
AU4	B_PERp5	I	Receiver differential pair, B Channels, Lane 5	
AT3	B_PERn5	I		
AP7	B_PERp6	I	Receiver differential pair, B Channels, Lane 6	
AR6	B_PERn6	I		
AU10	B_PERp7	I	Receiver differential pair, B Channels, Lane 7	
AT9	B_PERn7	I		
Reference Clock				
Y5	REFCLK+	I	100 MHz. Reference Clock (Differential Pair) to be used in Common Clock configuration, as defined by the *PCIe Base Specification*	
V5	REFCLK-	I		
Y19	REFCLK_Out+ (2)	O	100 MHz. This pin is used for driving REFCLK_out+.	
V19	REFCLK_Out1 (2)	O	100 MHz. This pin is used for driving REFCLK_out -.	
PCI Express Auxiliary Signals				
Y1	PERST#	I	Fundamental Reset; Active Low	1.8V (3.3V tolerant)
B11	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8V (3.3V tolerant)
JTAG				
AC18	JTAG_TDI	I	JTAG Test Data In	1.8V (3.3V tolerant)
L18	JATG_TDO	O	JTAG Test Data Out; Open drain; Require pull up on the platform; Pull up voltage must be selected based on the I/O voltage selected for other JTAG signals	
E16	JTAG_TMS	I	JTAG Test Mode Select	1.8V (3.3V tolerant)
AG18	JTAG_TCK	I	JTAG Clock	1.8V (3.3V tolerant)
R18	JTAG_TRST#	I	JTAG Reset; Active Low	1.8V (3.3V tolerant)
System Management Bus (SMBus)				
AC6	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8V (3.3V tolerant)
AG6	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8V (3.3V tolerant)
R6	SMB_ADDR_1	I	SMBus Address Bit 1	1.8V (3.3V tolerant)
L6	SMB_ADDR_2	I	SMBus Address Bit 2	1.8V (3.3V tolerant)
V23	SMB_ADDR_3/ VD_12	I	SMBus Address Bit 3or Vendor Defined	1.8V (3.3V tolerant)
EEPROM Configuration Interface				
AP11	EE_CLK/VD_5(1)	I/O	EEPROM Interface Clock or Vendor Defined	1.8V (3.3V tolerant)
AP13	EE_DAT/VD_6(1)	I/O	EEPROM Interface Data or Vendor Defined	1.8V (3.3V tolerant)

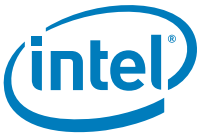


Table 3-2. x8 Retimer Signal Descriptions (Sheet 4 of 4)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
Miscellaneous				
AT1	VD_1	TBD	Vendor Defined Signal	
W2	VD_2	TBD	Vendor Defined Signal	
B1	VD_3	TBD	Vendor Defined Signal	
AU12	VD_4	TBD	Vendor Defined Signal	
D11	VD_7(1)	TBD	Vendor Defined Signal	
D13	VD_8(1)	TBD	Vendor Defined Signal	
A12	VD_9	TBD	Vendor Defined Signal	
W22	VD_10	TBD	Vendor Defined Signal	
AT23	VD_11	TBD	Vendor Defined Signal	
B23	VD_13	TBD	Vendor Defined Signal	
AT13	RX_DET_BYP	I	Receiver Detection Bypass	
Power				
16 pins	PWR_1	Power Rail 1	1.8V or 3.3V	
48 pins	PWR_2	Power Rail 2	1.1V or 1.0V or 0.9V or 0.8V	
175pins	GND		0V	

Notes:
1. It is safe to route high speed Vendor Defined signals at these locations. Rest VD pins are recommended to be used for static/ quasi static (low slew rate) signals. Routing high frequency signals on these may impose crosstalk on high-speed signals. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins.
2. REFCLK Out is compliant with REFCLK definition in the *PCIe Base Specification*.

3.6.1 Signal Descriptions

3.6.1.1 SMBus Interface

Refer to Section 3.1.1.1, “SMBus Interface” on page 17.

3.6.1.2 EEPROM Interface

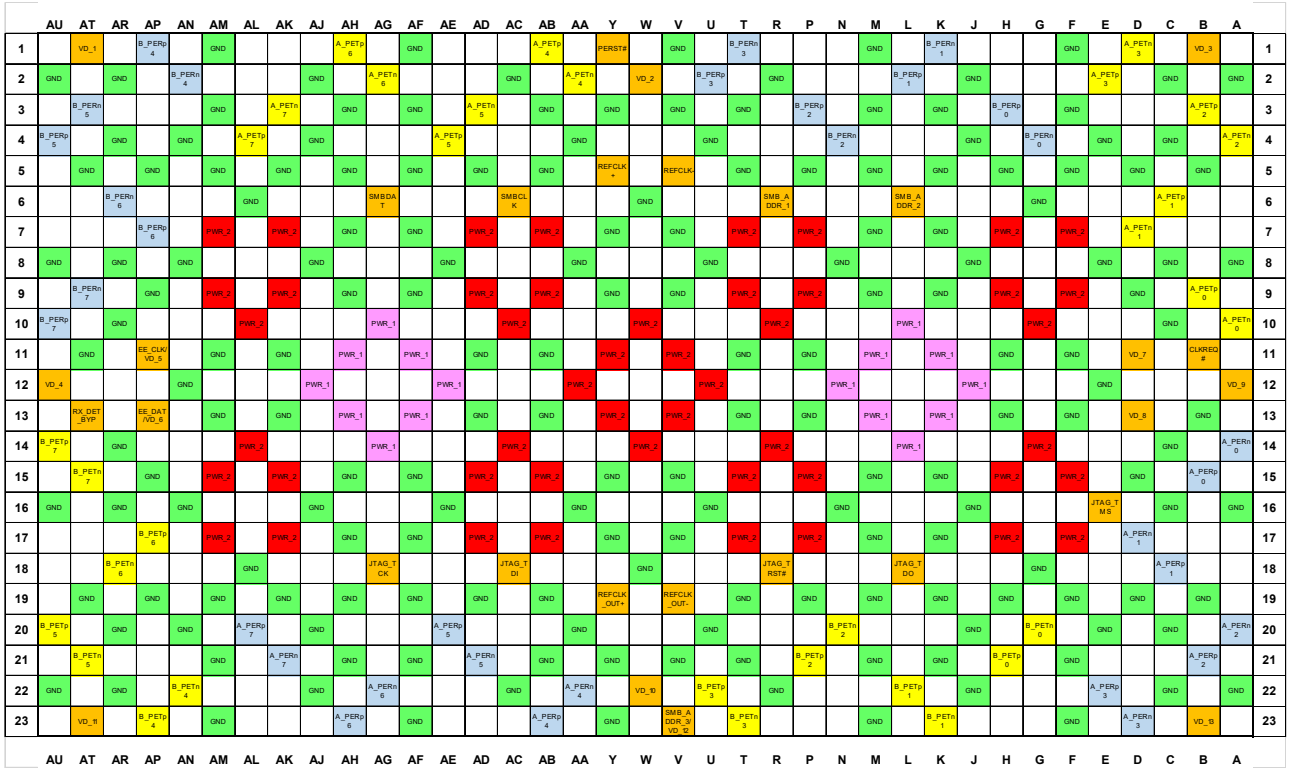
Refer to Section 3.1.1.2, “EEPROM Interface” on page 17

3.6.1.3 Miscellaneous Signals

Refer to Section 3.1.1.3, “Miscellaneous Signals” on page 17.

3.7 x8 Retimer Ballmap (Package Side)

Figure 3-6. x8 Retimer, Package-Side Pin Arrangement (Top View)



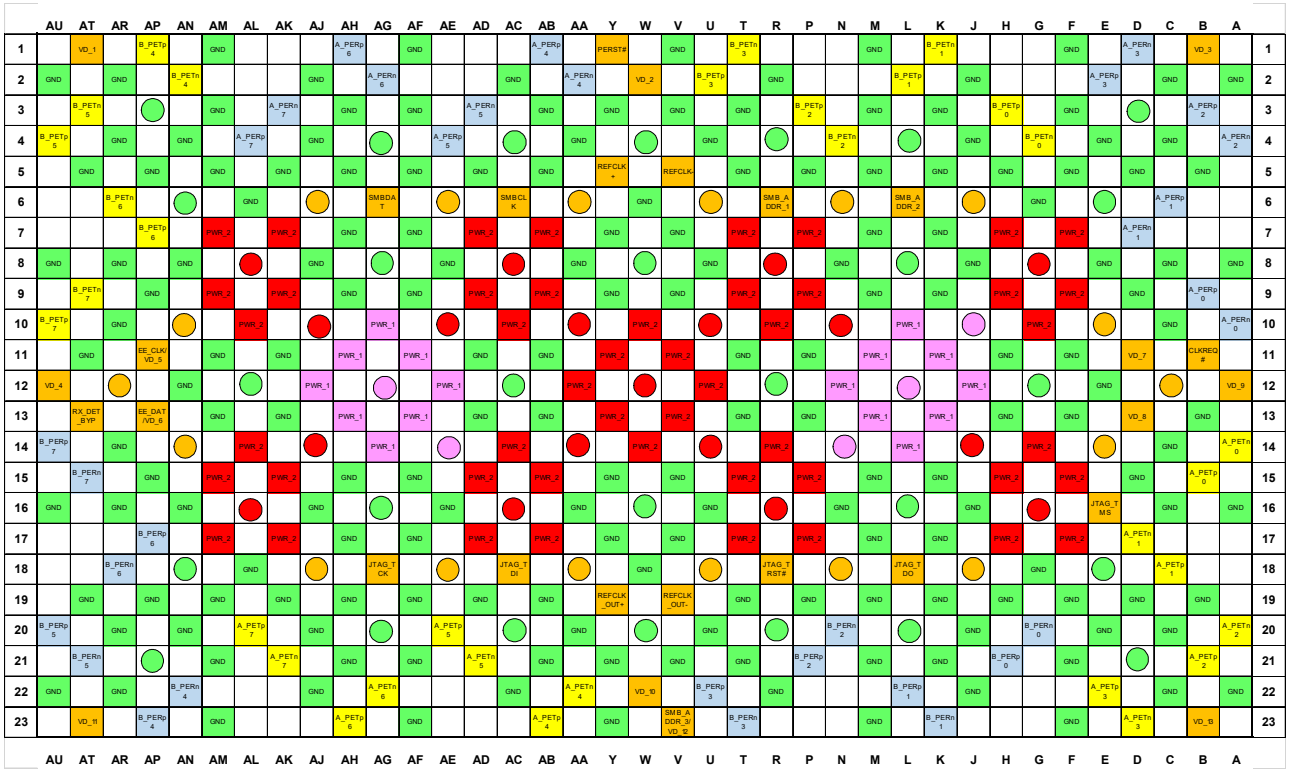
AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
	VD_1		B_PERp 4		GND				A_PETp 6		GND				A_PETp 4		PERST#		GND		B_PERn 3				GND		B_PERn 1				GND		A_PETn 3		VD_3		1
GND		GND		B_PERn 4				GND		A_PETn 6				GND		A_PETn 4		VD_2		B_PERp 3		GND				B_PERp 1		GND				A_PETp 3		GND		GND	2
	B_PERn 5				GND		A_PETn 7		GND		GND		A_PETn 5		GND		GND		GND		GND		B_PERp 2		GND		GND		B_PERp 0		GND				A_PETp 2		3
B_PERp 5		GND		GND		A_PETp 7		GND				A_PETp 5				GND				GND				B_PERn 2				GND		B_PERn 0		GND		GND		A_PETn 2	4
	GND		GND		GND		GND		GND		GND		GND		GND		REFCLK+		REFCLK-		GND		GND		GND		GND		GND		GND		GND		GND		5
		B_PERn 6				GND				SMBDAT				SMBCLK				GND				SMB_ADDR_1				SMB_ADDR_2				GND				A_PETp 1			6
			B_PERp 6		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		A_PETn 1					7
GND		GND		GND				GND				GND				GND				GND				GND				GND				GND		GND		GND	8
	B_PERn 7		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		A_PETp 0		9
B_PERp 7		GND				PWR_2				PWR_1				PWR_2				PWR_2				PWR_2				PWR_1				PWR_2				GND		A_PETn 0	10
	GND		EE_CLK/ VD_5		GND		GND		PWR_1		PWR_1		GND		GND		PWR_2		PWR_2		GND		GND		PWR_1		PWR_1		GND		GND		VD_7		CLKREQ#		11
VD_4				GND				PWR_1				PWR_1				PWR_2				PWR_2				PWR_1				PWR_1				GND				VD_9	12
	RX_DET_BYP		EE_DAT /VD_6		GND		GND		PWR_1		PWR_1		GND		GND		PWR_2		PWR_2		GND		GND		PWR_1		PWR_1		GND		GND		VD_8		GND		13
B_PETp 7		GND				PWR_2				PWR_1				PWR_2				PWR_2				PWR_2				PWR_1				PWR_2				GND		A_PERn 0	14
	B_PETn 7		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		A_PERp 0		15
GND		GND		GND				GND				GND				GND				GND				GND				GND				JTAG_TMS		GND		GND	16
			B_PETp 6		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		GND		GND		PWR_2		PWR_2		A_PERn 1					17
		B_PETn 6				GND				JTAG_TCK				JTAG_TDI				GND				JTAG_TRST#					JTAG_TDO				GND				A_PERp 1			18
	GND		GND		GND		GND		GND		GND		GND		GND		REFCLK_OUT+		REFCLK_OUT-		GND		GND		GND		GND		GND		GND		GND		GND		19
B_PETp 5		GND		GND		A_PERp 7		GND				A_PERp 5				GND				GND				B_PETn 2				GND		B_PETn 0		GND		GND		A_PERn 2	20
	B_PETn 5				GND		A_PERn 7		GND		GND		A_PERn 5		GND		GND		GND		GND		B_PETp 2		GND		GND		B_PETp 0		GND				A_PERp 2		21
GND		GND		B_PETn 4				GND		A_PERn 6				GND		A_PERn 4		VD_10		B_PETp 3		GND				B_PETp 1		GND				A_PERp 3		GND		GND	22
	VD_11		B_PETp 4		GND				A_PERp 6		GND				A_PERp 4		GND		SMB_ADDR_3/ VD_12		B_PETn 3				GND		B_PETn 1				GND		A_PERn 3		VD_13		23
AU	AT	AR	AP	AN	AM	AL	AK	AJ	AH	AG	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Legend	
	PWR_1
	PWR_2
	GND
	Control Signals
	Differential TX
	Differential RX
	No Balls

3.8 X8 Retimer Ballmap (Platform Side)

The following figure shows the platform side land pattern. The TX and RX balls have been swapped when compared to package side ballmap, i.e., "TX lane x" in package side ballmap gets mapped to "RX lane x" in the land pattern.

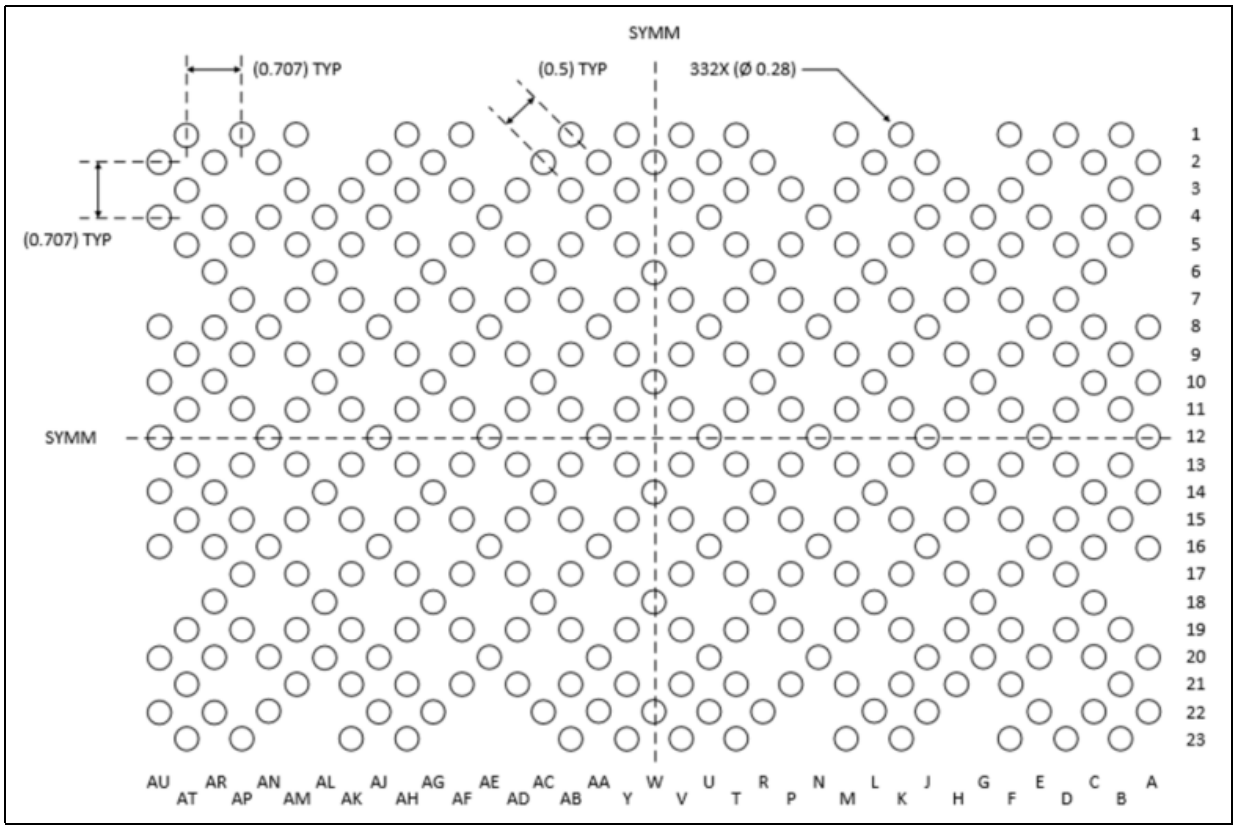
Figure 3-7. x8 Retimer, Platform-Side Pin Arrangement (Top View)



Legend	
	PWR_1 Via
	PWR_2 Via
	GND Via
	Control Signal Via

3.9 x8 Retimer, Physical Ballmap (Package Side)

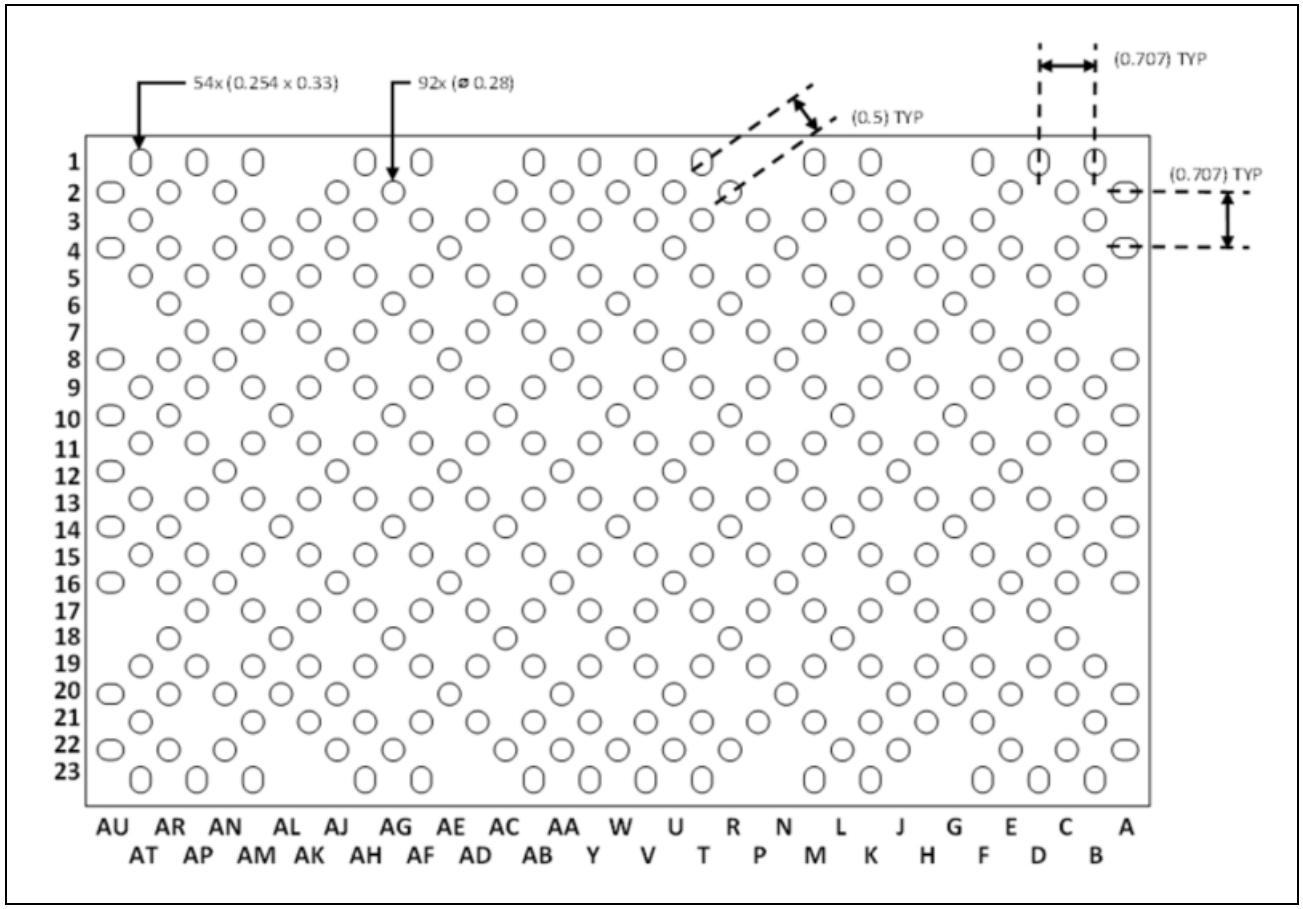
Figure 3-8. x8 Retimer, Physical Ballmap on Package (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.10 x8 Retimer Platform Side Land Pattern

Figure 3-9. x8 Retimer, Platform-Side Land Pattern with Spacing Details (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.11 x4 Retimer Interface Signals

Table 3-3. x4 Retimer Signal Descriptions (Sheet 1 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
High Speed Differential I/Os				
A3	A_PETp0	O	Transmitter differential pair, A Channels, Lane 0	
A4	A_PETn0	O		
C1	A_PETp1	O	Transmitter differential pair, A Channels, Lane 1	
B1	A_PETn1	O		
F1	A_PETp2	O	Transmitter differential pair, A Channels, Lane 2	
E1	A_PETn2	O		

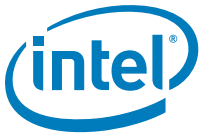


Table 3-3. x4 Retimer Signal Descriptions (Sheet 2 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
J1	A_PETp3	O	Transmitter differential pair, A Channels, Lane 3	
H1	A_PETn3	O		
A8	A_PERp0	I	Receiver differential pair, A Channels, Lane 0	
A7	A_PERn0	I		
C10	A_PERp1	I	Receiver differential pair, A Channels, Lane 1	
B10	A_PERn1	I		
F10	A_PERp2	I	Receiver differential pair, A Channels, Lane 2	
E10	A_PERn2	I		
J10	A_PERp3	I	Receiver differential pair, A Channels, Lane 3	
H10	A_PERn3	I		
M10	B_PETp0	O	Transmitter differential pair, B Channels, Lane 0	
I10	B_PETn0	O		
R10	B_PETp1	O	Transmitter differential pair, B Channels, Lane 1	
P10	B_PETn1	O		
V10	B_PETp2	O	Transmitter differential pair, B Channels, Lane 2	
U10	B_PETn2	O		
W7	B_PETp3	O	Transmitter differential pair, B Channels, Lane 3	
W8	B_PETn3	O		
M1	B_PERp0	I	Receiver differential pair, B Channels, Lane 0	
L1	B_PERn0	I		
R1	B_PERp1	I	Receiver differential pair, B Channels, Lane 1	
P1	B_PERn1	I		
V1	B_PERp2	I	Receiver differential pair, B Channels, Lane 2	
U1	B_PERn2	I		
W4	B_PERp3	I	Receiver differential pair, B Channels, Lane 3	
W3	B_PERn3	I		
Reference Clock				
C5	REFCLK+	I	100 MHz. Reference Clock (Differential Pair) to be used in Common Clock configuration, as defined by the *PCIe Base Specification*	
C6	REFCLK-	I		
U5	REFCLK_Out+ (2)	O	100 MHz. This pin is used for driving REFCLK_out+.	
U6	REFCLK_Out- (2)	O	100Mhz. This pin is used for driving REFCLK_out-.	
PCI Express Auxiliary Signals				
A2	PERST#	I	Fundamental Reset; Active Low	1.8V (3.3V tolerant)
A9	CLKREQ#	I	Used by L1PM Substates; Active Low	1.8V (3.3V tolerant)
JTAG				
U3	JTAG_TDI	I	JTAG Test Data In	1.8V (3.3V tolerant)
C3	JATG_TDO	O	JTAG Test Data Out; Open drain; Require pull up on the platform; Pull up voltage must be selected based on the I/O voltage selected for other JTAG signals	

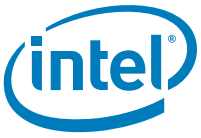
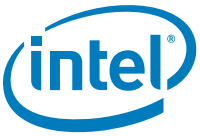


Table 3-3. x4 Retimer Signal Descriptions (Sheet 3 of 3)

Pin#	Signal Name	Signal Direction	Signal Description	Voltage Level
N3	JTAG_TMS	I	JTAG Test Mode Select	1.8V (3.3V tolerant)
K3	JTAG_TCK	I	JTAG Clock	1.8V (3.3V tolerant)
G3	JTAG_TRST#	I	JTAG Reset; Active Low	1.8V (3.3V tolerant)
System Management Bus (SMBus)				
G8	SMBCLK	I/O	SMBus Clock Input / Open Drain Clock Output	1.8V (3.3V tolerant)
K8	SMBDAT	I/O	SMBus Data Input / Open Drain Output	1.8V (3.3V tolerant)
W5	SMB_ADDR_1	I	SMBus Address Bit 1	1.8V (3.3V tolerant)
W6	SMB_ADDR_2	I	SMBus Address Bit 2	1.8V (3.3V tolerant)
W9	SMB_ADDR_3/ VD_10	I	SMBus Address Bit 3 or Vendor Defined	1.8V (3.3V tolerant)
EEPROM Configuration Interface				
U8	EE_DAT/VD_7(1)	I/O	EEPROM Interface Data or Vendor Defined	1.8V (3.3V tolerant)
N8	EE_CLK/VD_8(1)	I/O	EEPROM Interface Clock or Vendor Defined	1.8V (3.3V tolerant)
Miscellaneous				
W1	VD_1	TBD	Vendor Defined Signal	
W2	VD_2	TBD	Vendor Defined Signal	
W10	VD_3	TBD	Vendor Defined Signal	
A1	VD_4	TBD	Vendor Defined Signal	
A5	VD_5	TBD	Vendor Defined Signal	
A10	VD_6	TBD	Vendor Defined Signal	
C8	VD_9	TBD	Vendor Defined Signal	
A6	RX_DET_BYP	I	Receiver Detection Bypass	
Power				
5 pins	PWR_1	Power Rail 1	3.3V or 1.8V	
29 pins	PWR_2	Power Rail 2	1.1V or 1.0V or 0.9V or 0.8V	
54 pins	GND		0 V	

Notes:
1. It is safe to route high speed Vendor Defined signals at these locations. Rest VD pins are recommended to be used for static/ quasi static (low slew rate) signals. Routing high frequency signals on these may impose crosstalk on high-speed signals. Retimer vendors are recommended to do a thorough signal integrity analysis when using any of the VD pins.
2. REFCLK Out is compliant with REFCLK definition in the *PCIe Base Specification*.



3.11.1 Signal Descriptions

3.11.1.1 SMBus Interface

Refer to Section 3.1.1.1, "SMBus Interface" on page 17.

3.11.1.2 EEPROM Interface

Refer to Section 3.1.1.2, "EEPROM Interface" on page 17

3.11.1.3 Miscellaneous Signals

Refer to Section 3.1.1.3, "Miscellaneous Signals" on page 17.

3.12 x4 Retimer Ballmap (Package Side)

Figure 3-10. x4 Retimer, Package-Side Pin Arrangement (Top View)

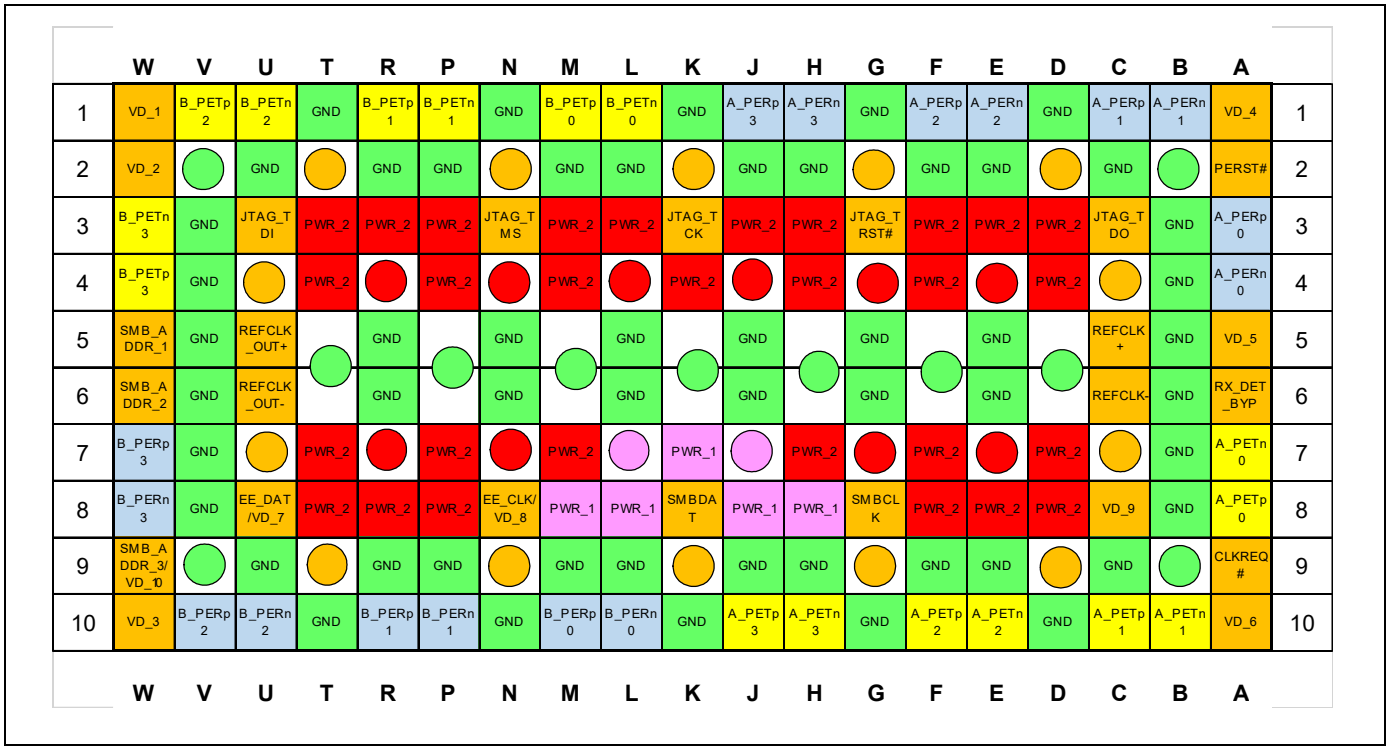
	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	VD_1	B_PERp 2	B_PERn 2	GND	B_PERp 1	B_PERn 1	GND	B_PERp 0	B_PERn 0	GND	A_PETp 3	A_PETn 3	GND	A_PETp 2	A_PETn 2	GND	A_PETp 1	A_PETn 1	VD_4	1
2	VD_2		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		PERST#	2
3	B_PERn 3	GND	JTAG_T DI	PWR_2	PWR_2	PWR_2	JTAG_T MS	PWR_2	PWR_2	JTAG_T CK	PWR_2	PWR_2	JTAG_T RST#	PWR_2	PWR_2	PWR_2	JTAG_T DO	GND	A_PETp 0	3
4	B_PERp 3	GND		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		GND	A_PETn 0	4
5	SMB_A DDR_1	GND	REFCLK _OUT+		GND		GND		GND		GND		GND		GND		REFCLK +	GND	VD_5	5
6	SMB_A DDR_2	GND	REFCLK _OUT-		GND		GND		GND		GND		GND		GND		REFCLK-	GND	RX_DET _BYP	6
7	B_PETp 3	GND		PWR_2		PWR_2		PWR_2		PWR_1		PWR_2		PWR_2		PWR_2		GND	A_PERn 0	7
8	B_PETn 3	GND	EE_DAT /VD_7	PWR_2	PWR_2	PWR_2	EE_CLK/ VD_8	PWR_1	PWR_1	SMBDA T	PWR_1	PWR_1	SMBCL K	PWR_2	PWR_2	PWR_2	VD_9	GND	A_PERp 0	8
9	SMB_A DDR_3/ VD_10		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		CLKREQ #	9
10	VD_3	B_PETp 2	B_PETn 2	GND	B_PETp 1	B_PETn 1	GND	B_PETp 0	B_PETn 0	GND	A_PERp 3	A_PERn 3	GND	A_PERp 2	A_PERn 2	GND	A_PERp 1	A_PERn 1	VD_6	10
	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Legend	
	PWR_1
	PWR_2
	GND
	Control Signals
	Differential TX
	Differential RX
	No Balls

3.13 x4 Retimer Ballmap (Platform Side)

The following figure shows the platform side land pattern. The TX and RX balls have been swapped when compared to package side ballmap, i.e., "TX lane x" in package side ballmap gets mapped to "RX lane x" in the land pattern.

Figure 3-11. x4 Retimer, Platform-Side Land Pattern (Top View)

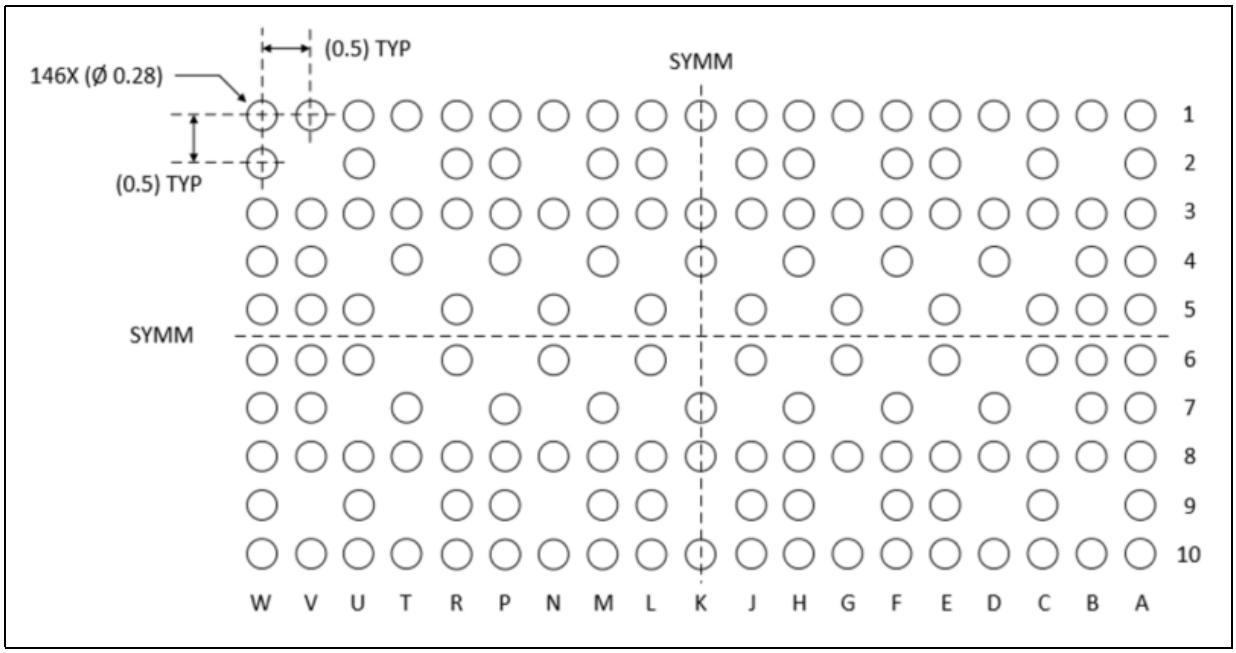


	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	VD_1	B_PETp 2	B_PETn 2	GND	B_PETp 1	B_PETn 1	GND	B_PETp 0	B_PETn 0	GND	A_PERp 3	A_PERn 3	GND	A_PERp 2	A_PERn 2	GND	A_PERp 1	A_PERn 1	VD_4	1
2	VD_2		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		PERST#	2
3	B_PETn 3	GND	JTAG_TDI	PWR_2	PWR_2	PWR_2	JTAG_TMS	PWR_2	PWR_2	JTAG_TCK	PWR_2	PWR_2	JTAG_TRST#	PWR_2	PWR_2	PWR_2	JTAG_TDO	GND	A_PERp 0	3
4	B_PETp 3	GND		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		PWR_2		GND	A_PERn 0	4
5	SMB_ADDR_1	GND	REFCLK_OUT+		GND		GND		GND		GND		GND		GND		REFCLK+	GND	VD_5	5
6	SMB_ADDR_2	GND	REFCLK_OUT-		GND		GND		GND		GND		GND		GND		REFCLK-	GND	RX_DET_BYP	6
7	B_PERp 3	GND		PWR_2		PWR_2		PWR_2		PWR_1		PWR_2		PWR_2		PWR_2		GND	A_PETn 0	7
8	B_PERn 3	GND	EE_DAT/VD_7	PWR_2	PWR_2	PWR_2	EE_CLK/VD_8	PWR_1	PWR_1	SMBDAT	PWR_1	PWR_1	SMBCLK	PWR_2	PWR_2	PWR_2	VD_9	GND	A_PETp 0	8
9	SMB_ADDR_3/VD_10		GND		GND	GND		GND	GND		GND	GND		GND	GND		GND		CLKREQ#	9
10	VD_3	B_PERp 2	B_PERn 2	GND	B_PERp 1	B_PERn 1	GND	B_PERp 0	B_PERn 0	GND	A_PETp 3	A_PETn 3	GND	A_PETp 2	A_PETn 2	GND	A_PETp 1	A_PETn 1	VD_6	10
	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Legend	
	PWR_1 Via
	PWR_2 Via
	GND Via
	Control Signal Via

3.14 x4 Retimer, Physical Ballmap (Package Side)

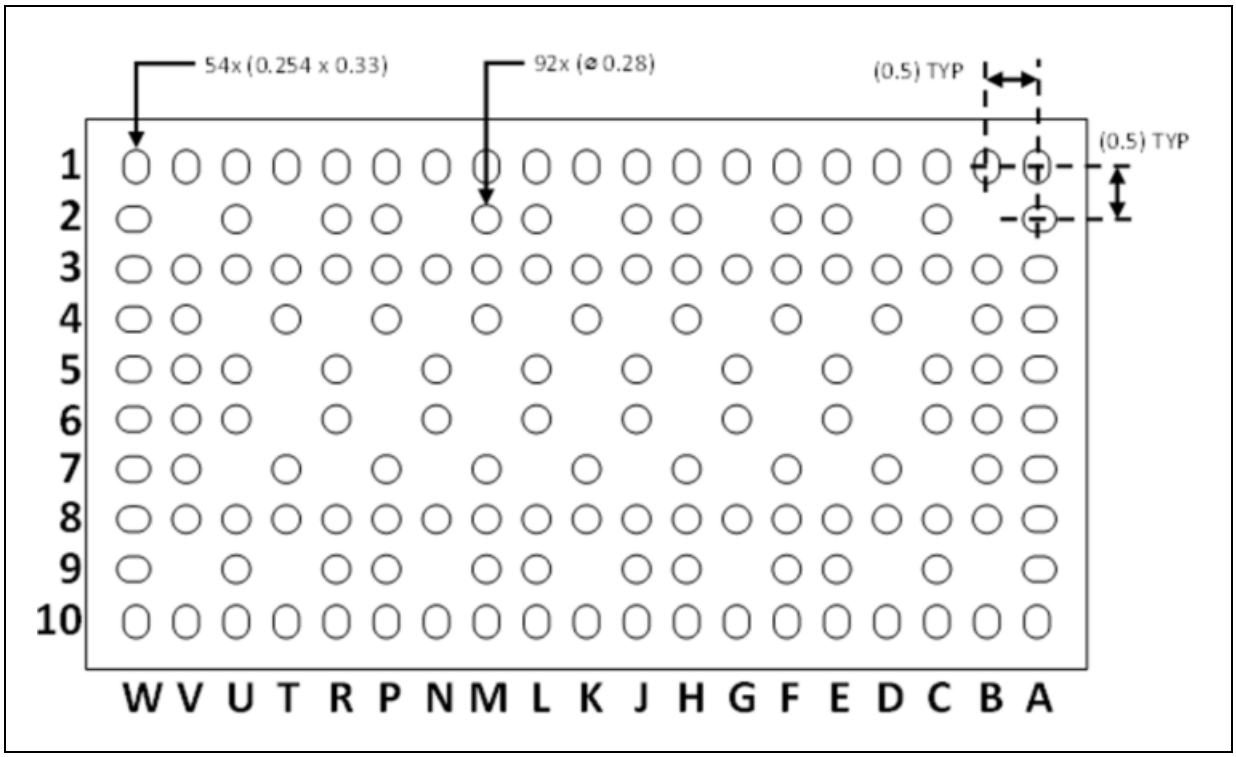
Figure 3-12. x4 Retimer, Physical Ballmap on Package (Top View)



Note: All dimensions are in mm and all distances are center to center.

3.15 X4 Retimer Platform Side Land Pattern

Figure 3-13. x4 Retimer, Platform-Side Land Pattern with Spacing Details (Top View)



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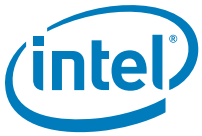


4 Electrical Characteristics

Two power supplies are supported, PWR_1 and PWR_2.

PWR_1 supports 3.3V or 1.8V. PWR_2 supports one of (0.8V, 0.9V, 1.0V, 1.1V). Actual voltage is to be decided between retimer vendor and the system vendor.

PWR_1 rail is intended for control signals and sideband signals, whereas PWR_2 is intended for high-speed signaling.

Table 4-2 lists power distribution for the two rails (PWR_1 and PWR_2) for x4, x8 and x16 configurations.

4.1 Absolute Maximum Ratings

The following table lists the absolute maximum supply voltage ratings.

Table 4-1. Absolute Maximum Voltage Ratings

Symbol	Parameter	Min.	Max.	Units	Notes
3.3V	3.3V Supply Voltage	2.8	3.6	V	1
1.8V	1.8V Supply Voltage	1.7	1.9	V	1
1.1V	1.1V Supply Voltage	1.06	1.17	V	1
1.0V	1.0V Supply Voltage	0.95	1.1	V	1
0.9V	0.9V Supply Voltage	0.86	0.98	V	1
0.8V	0.8V Supply Voltage	0.76	0.87	V	1

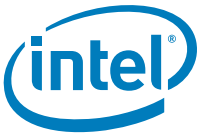
Note:
1. No specific power-on and power-off sequence is required for various supply voltage rails.

4.2 Power Consumption

The following table lists power consumption values under maximum operating conditions. Maximum power is consumed while all the lanes are operating at 16 GT/s with full swing on the transmitter. Refer to Section 4.5 for details of thermal requirements.

Table 4-2. Recommended Absolute Maximum Power Ratings

	Power_1	Power_2	Unit
x16	1.7	6.8	W
x8	0.85	3.4	W
x4	0.425	1.7	W



4.3 Power Supply Decoupling

Due to the low level signaling of the PCI Express interface, it is recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote upstream PCI Express device. Some basic guidelines to help ensure a quiet power supply are provided below.

Note: The following are guidelines only. It is the responsibility of the retimer designer and the platform designer to properly test the design to ensure that retimer circuitry does not create excessive noise on power supply or ground signals at the retimer package balls.

- For PWR_1 rail, a bulk decoupling capacitor of value 1x470 uF (aluminum) and 1x22 uF (0805) is recommended near VR on the platform.
- For PWR_1 rail, 1x10 uF (0603) capacitor is recommended at top cavity on the platform.
- For PWR_1 rail, 1x10 uF (0603) capacitor is recommended at bottom cavity on the platform.
- For PWR_2 rail, a bulk decoupling capacitor of value 1x470 uF (aluminum) and 1x22 uF (0805) is recommended near VR on the platform.
- For PWR_2 rail, 2x10 uF (0603) capacitors and 1x10 uF (0805) capacitor is recommended at the top cavity on the platform.
- For PWR_2 rail, 1x22 uF (0805) capacitor is recommended at the bottom cavity on the platform.
- It is recommended that the retimer vendor incorporate the decoupling caps in the package or in the die as needed to minimize noise at the package balls.

4.4 Retimer Latency

The maximum latency (refer to the base specification) specification for PCIe 4.0 retimers is 64 ns to 91 ns depending on clocking architecture and maximum payload size. Some applications may need significantly lower latency (less than 10 ns). OEMs are recommended to work with retimer vendors for this low latency use case.

4.5 Package Thermal Considerations

Parameter	Description	Value	Units
$T_{J(max)}$	Junction temperature	125	°C
$T_{A(max)}$	Ambient temperature	85	°C

Detailed thermal analysis including heat sink requirements are outside the scope of this specification. The retimers will be used in a variety of chassis types/Platforms. It is up to the retimer vendor and the OEM to figure out thermal/heatsink requirements based on the chassis type and specific location on the chassis for the retimer.

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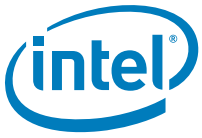

5 SMBus and EEPROM

It is recommended that each retimer have a dedicated EEPROM behind it from where the retimer loads its configuration data upon power up. A dedicated EEPROM interface allows retimer to use fixed address to access the EEPROM.

It is recommended that the retimer load the configuration through EEPROM. Once the EEPROM configuration is loaded, if any additional configuration changes are needed, it is done using SMBus interface from the platform side.

If the retimer is located on a CEM riser card, it is not possible for platform to program the retimer using SMBus interface as the platform does not know the retimer address. In that case, the retimer (located on CEM riser card) is required to have a dedicated EEPROM associated with it. It should be noted that, once the retimer loads configuration from this EEPROM, it cannot be changed using SMBus commands from the platform.

Retimer pinout supports 3 SMBus address pins allowing up to 8 addressable devices on the bus. If more than 8 devices (and hence addresses) are needed, some kind of SMBus multiplexing is to be used on the platform side. Details of how SMBus multiplexing and addressing is done on the platform is left to be implementation specific.

It is recommended to minimize the configurations through SMBus in applications where boot time is to be minimized.

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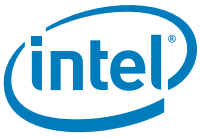


6 BGA Footprint Register Configuration

6.1 SMBus Address Range

Retimer SMBus address will be chosen from the range 20h to 27h.

The following tables hows the bit level mapping for the SMBus address byte.

Table 6-1. SMBus Address bits Mapping

Address Bit	Address Bit Value
1	SMB_ADDR_1
2	SMB_ADDR_2
3	SMB_ADDR_3
4	0
5	1
6	0
7	0

6.2 SMBus Command Formats

The SMBus interface responds to following SMBus commands.

Refer to the SMBus specification for a detailed description of these commands.

Block Write/Read with PEC.

The following figure defines the command code associated with retimer SMBus transactions.

Figure 6-1. Slave SMBus Command Code Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PEC	RSVD		FUNCTION			START	END

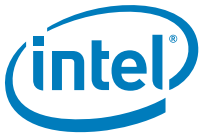


Table 6-2. Slave SMBus Command Code Fields

Bit Field	Name	Description
0	END	End of transaction indicator. Setting both START and END signifies a single transaction sequence. 0 = Current transaction is not the last read or write sequence. 1 = Current transaction is the last read or write sequence. Refer to Table 6-3 for usage of this bit.
1	START	Start of transaction indicator. Setting both START and END signifies a single transaction sequence. 0 = Current transaction is not the first of a read or write sequence. 1 = Current transaction is the first of a read or write sequence. Refer to Table 6-3 for usage of this bit.
4:2	FUNCTION	This field encodes the type of SMBus operation. 000 - Retimer register read operation 001 - Retimer register write operation 010 - Vendor defined 011 - Vendor defined 100 - Vendor defined 101 - Vendor defined 110 - Vendor defined 111 - Vendor defined
6:5	RSVD	This field is Reserved.
7	PEC	This bit controls whether packet error checking is enabled for the current SMBus transaction. 0 = Packet error checking disabled for the current SMBus transaction. 1 = Packet error checking enabled for the current SMBus transaction.

START (Bit Field 1) and END (Bit Field 0) is used to indicate if the SMBus command spans across multiple transactions.

Table 6-3. START and END Bit Usage for Command Code

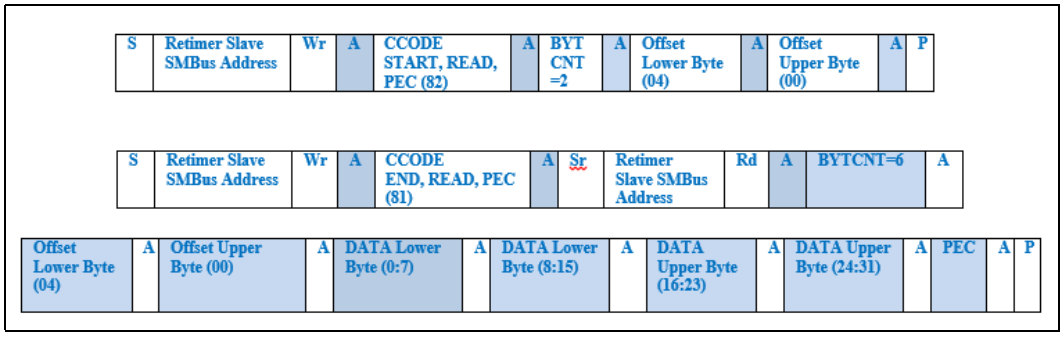
START Bit Value	END Bit Value	Description
1	0	This is the first transaction in a command that spans across multiple transactions.
0	1	This is the last transaction in a command that spans across multiple transactions.
1	1	The SMBus command is implemented using a single transaction.
0	0	Reserved

6.3 SMBus Block Read/Write Examples

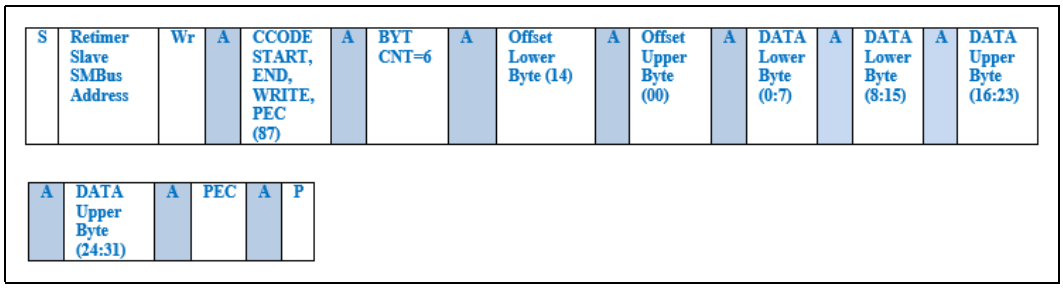
All read and write accesses to the registers should be 32 bits as shown in the examples below.

Non- shaded items in the examples are driven by SMBus host and shaded items are driven by SMBus Slave implementation on the retimer.

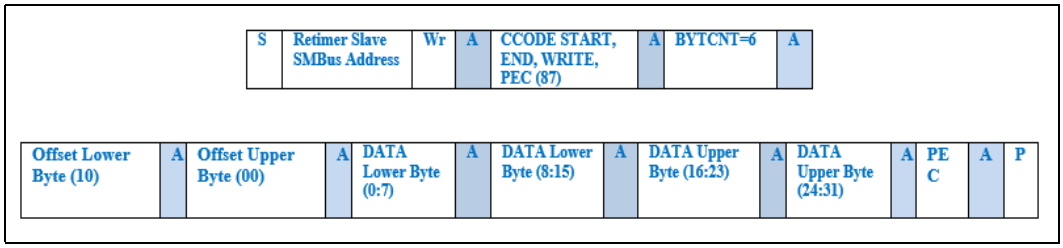
6.3.1 Read Vendor ID (Implemented Using Block Read with Repeat START)



6.3.2 Write 16G Preset (P7) for Downstream Pseudo Port



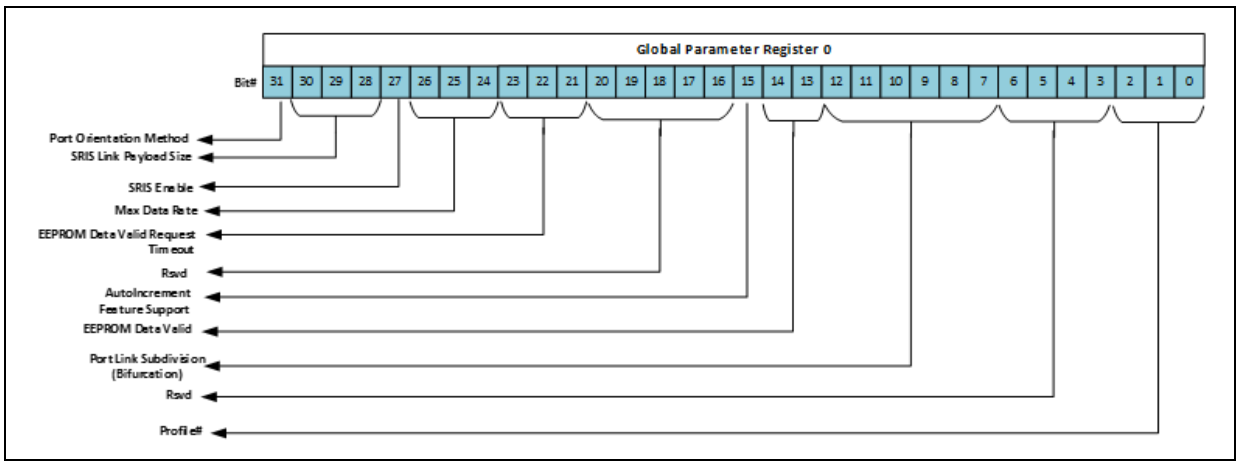
6.3.3 Enable SRIS (Implemented Using Block Write with Repeat START)



If the retimer sends NACK for any of the commands because it is not ready to write or read the data from specified offset location, the entire command needs to be repeated.

If the retimer supports the optional auto-increment feature, it can indicate the support by using a bit in the Global Parameter Register 0.

6.4 Global Parameter Register 0



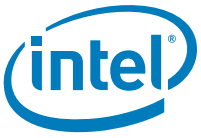


Table 6-4. Global Parameter Register 0 Description

Bit Location	Register Description	Attributes
2:0	**Profile#** This field indicates which retimer common footprint specification revision the retimer is implementing. 000: Rev 0.5 001: Rev 0.7+ (indicating this version of specification) 010:111 Reserved for future versions	RO
6:3	Rsvd	RO
12:7	**Port Link Subdivision (Bifurcation)** 000000: x16 000001: x8 000010: x4 000011: x8x8 000100: x8x4x4 000101: x4x4x8 000110: x4x4x4x4 000111: x2x2x2x2x2x2x2x2 001000: x8x4x2x2 001001: x8x2x2x4 001010: x2x2x4x8 001011: x4x2x2x8 001100: x2x2x2x2x8 001101: x8x2x2x2x2 001110: x2x2x4x4x4 001111: x4x2x2x4x4 010000: x4x4x2x2x4 010001: x4x4x4x2x2 010010: x2x2x2x2x4x4 010011: x2x2x4x4x2x2 010100: x4x2x2x2x2x4 010101: x2x2x4x4x2x2 010110: x4x2x2x4x2x2 010111: x4x4x2x2x2x2 011000: x2x2x2x2x2x2x4 011001: x2x2x2x2x4x2x2 011010: x2x2x4x2x2x2x2 011011: x4x2x2x2x2x2x2 011100: x4x4 011101: x2x2x4 011110: x4x2x2 011111: x2x2x2x2 100000: x2x2 100001:111111:Rsvd	RW
14:13	**EEPROM Data Valid** 00: No EEPROM 01: EEPROM Present and Data Valid 01: EEPROM Present and Data Not Valid 11: Controller Busy*	
15	**AutoIncrement Feature Support** 1: Supported 0: Not Supported	
20:16	Rsvd	RO

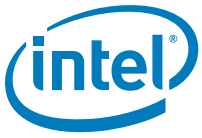


Table 6-4. Global Parameter Register 0 Description

Bit Location	Register Description	Attributes
23:21	**EEPROM Data Valid Request Timeout** 000: No delay 001: 10ms(Def) 010: 20ms 011: 30ms 100: 40ms 101: 50ms 110: 60ms 111: 70ms	RO
26:24	**Max Data Rate** 000: Rsvd 001: 2.5 G (Def) 010: 5.0 G 011: 8.0 G 100: 16 G 101: Rsvd 110: Rsvd 111: Rsvd	RW
27	**SRIS Enable** 0 = Common Clock (Def) 1 = SRIS	RW
30:28	**SRIS Link Payload Size** (valid when Bit3=1) 000: 128 001: 256 010: 512 011: 1024 100: 2048 101: 4096 (Def) 110: Rsvd 111: Rsvd	RW
31	**Port Orientation Method** 0 = Static 1 = Dynamic (Def)	RW

Note: *: If the BIOS reads this value, then the retimer controller is busy calculating the validity of the EEPROM data. The BIOS should retry after a timeout value specified in Global Parameter Register 0 (Bits [23:21], EEPROM Data Valid Request Timeout).

6.5 Global Parameter Register 1

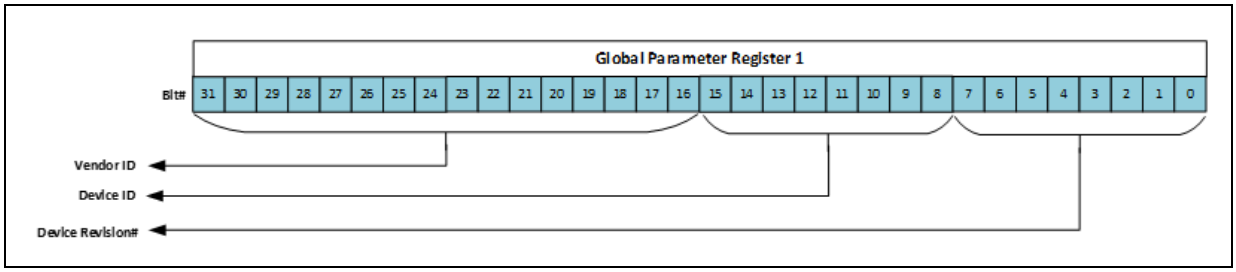


Table 6-5. Global Parameter Register 1 Description

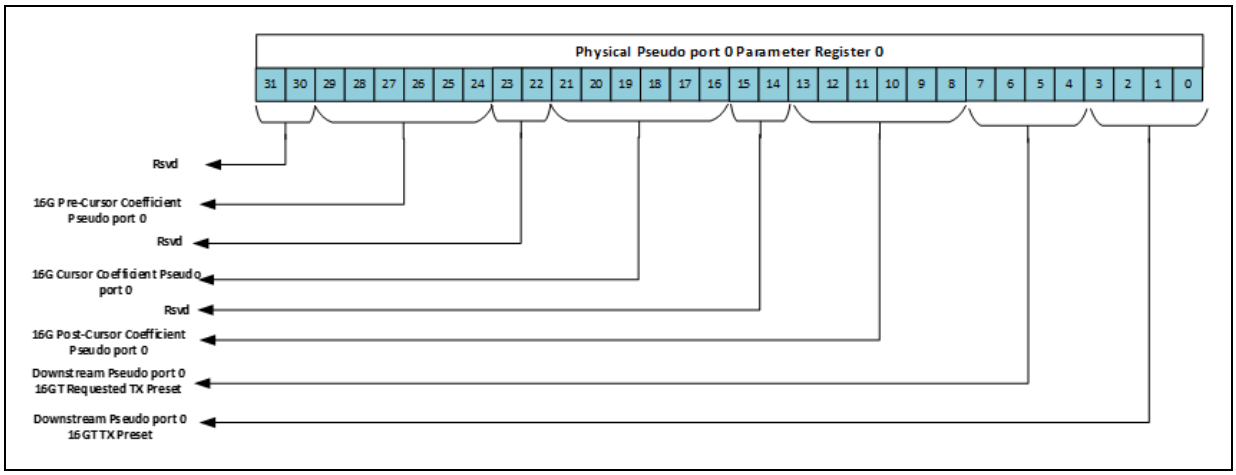
Bit Location	Register Description	Attributes
7:0	Device Revision #	RO
15:8	Device ID	RO
31:16	Vendor ID	RO

Vendor ID field identifies manufacturer of the device. This field contains the PCI-SIG* assigned vendor ID.

Device ID field value is chosen by the vendor.

Device Revision# value is chosen by retimer vendor. This value can be viewed as extension of the Device ID field.

6.6 Physical Pseudo Port 0 Parameter Register 0



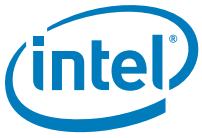


Table 6-6. Physical Pseudo Port 0 Parameter Register 0 Description

Bit Location	Register Description	Attributes
3:0	**Downstream Pseudo Port 0 16GT Tx Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	**Downstream Pseudo Port 0 16GT Tx Requested Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
13:8	16G Post-Cursor Coefficient Pseudo port 0 Coefficient 1 to Coefficient 64	RW
15:14	Reserved	RO
21:16	16G Cursor Coefficient Pseudo port 0 Coefficient 1 to Coefficient 64	RW
23:22	Reserved	R0
29:24	16G Pre-Cursor Coefficient Pseudo port 0 Coefficient 1 to Coefficient 64	RW
31:30	Reserved	R0

6.7 Physical Pseudo Port 0 Parameter Register 1

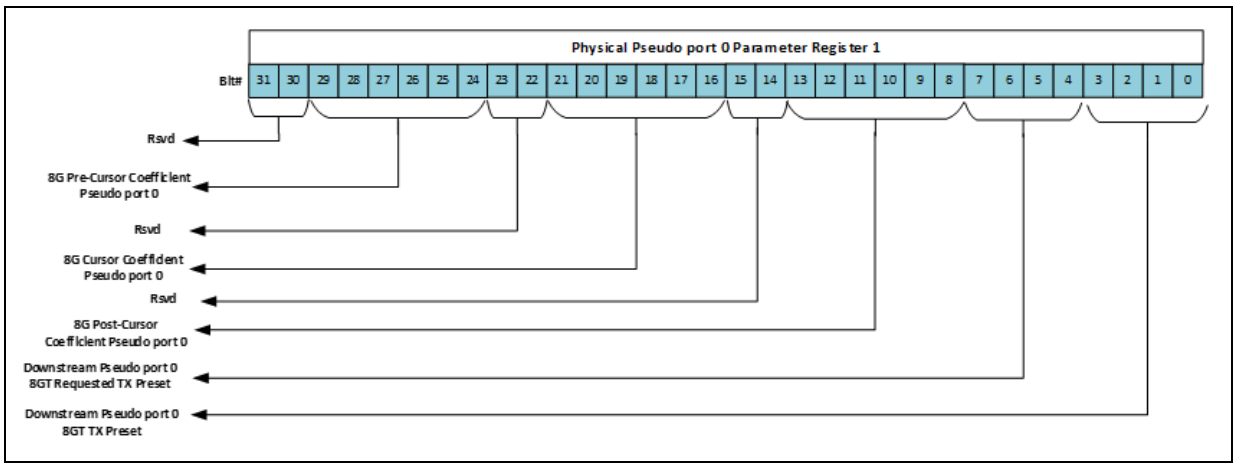


Table 6-7. Physical Pseudo Port 0 Parameter Register 1

Bit Location	Register Description	Attributes
3:0	**Downstream Pseudo Port 0, 8 GT/s TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	**Downstream Pseudo Port 08GT Requested TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
13:8	8G Post-Cursor Coefficient Pseudo port 0 Coefficient 1 to Coefficient 64	RW
15:14	Reserved	RO
21:16	8G Cursor Coefficient Pseudo port 0 Coefficient 1 to Coefficient 64	RW

Table 6-7. Physical Pseudo Port 0 Parameter Register 1

Bit Location	Register Description	Attributes
23:22	Reserved	RO
29:24	8G Pre-Cursor Coefficient Pseudo port 0 Coefficient 1 to Coefficient 64	RW
31:30	Reserved	RO

6.8 Physical Pseudo Port 0 Parameter Register 2

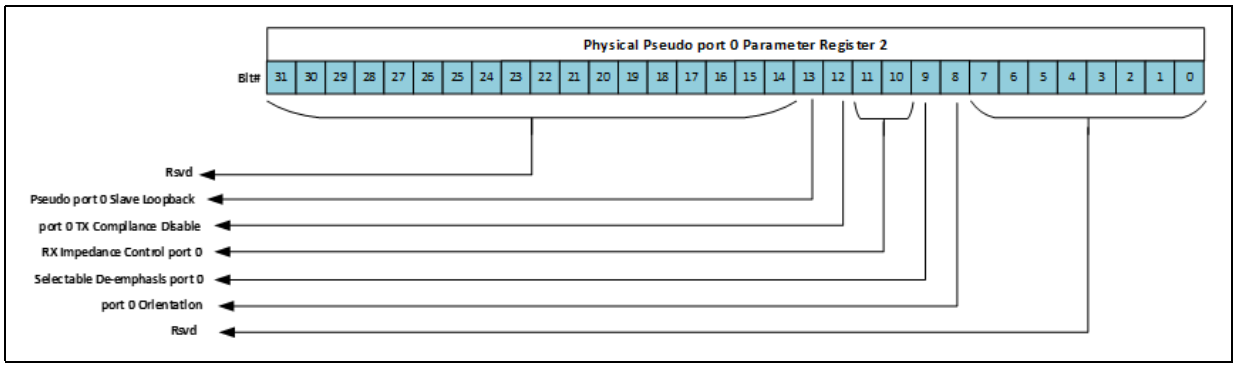


Table 6-8. Physical Pseudo Port 0 Parameter Register 2

Bit Location	Register Description	Attributes
7:0	Reserved	RO
8	**Port 0 Orientation** (valid when Port Orientation Method in Global Parameter Register = 0) 0 = Upstream (Def) 1 = Downstream	RO
9	**Selectable De-emphasis Port 0** 0 = -3.5 dB (Def) 1 = -6.0 dB	RW
11:10	**RX Impedance Control Port 0** 00: Static- On 01: Static- Off 10: Dynamic (Def) 11: Rsvd	RO
12	**Port 2TX Compliance Disable** 1 = Disable 0 = Enable (Def)	RW
13	**Pseudo Port 2 Slave Loopback** 1 = Enable 0 = Disable (Def)	RW
31:14	Reserved	RO

6.9 Physical Pseudo Port 1 Parameter Register 0

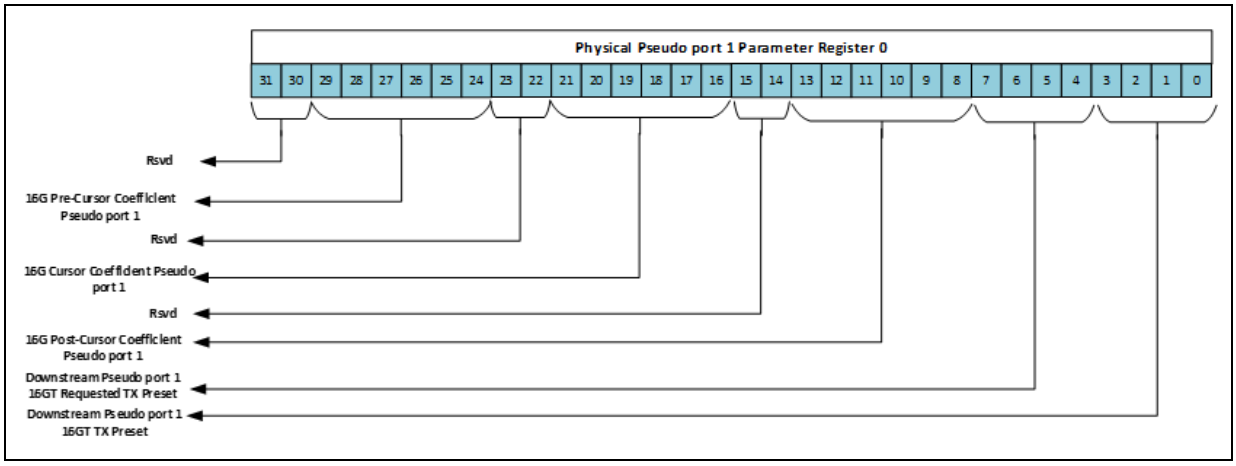


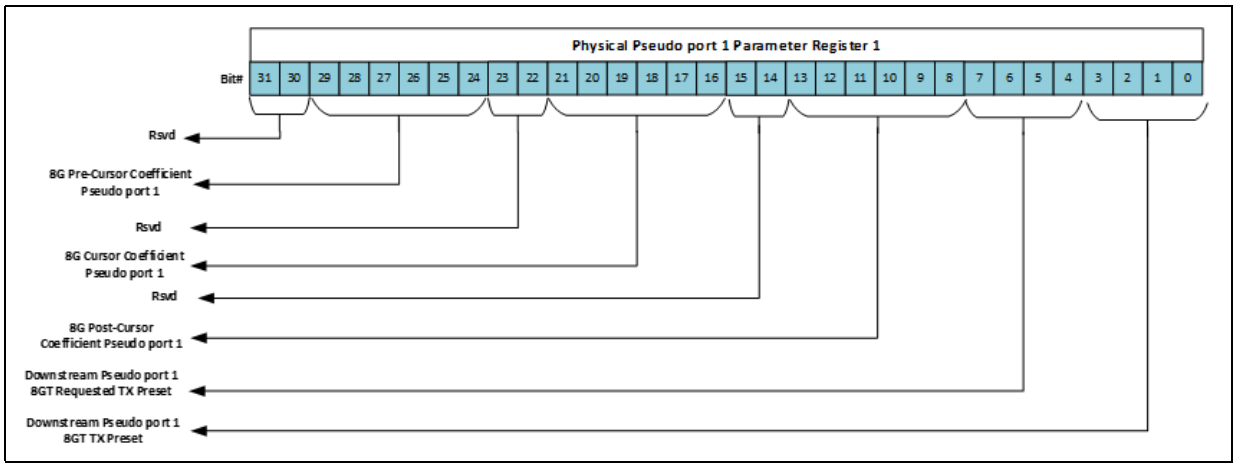
Table 6-9. Physical Pseudo Port 1 Parameter Register 0

Bit Location	Register Description	Attributes
3:0	**Downstream Pseudo Port 1 16GT Tx Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	**Downstream Pseudo Port 1 16GT Requested Tx Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
13:8	16G Post-Cursor Coefficient Pseudo port 1 Coefficient 1 to Coefficient 64	RW
15:14	Reserved	RO
21:16	16G Cursor Coefficient Pseudo port 1 Coefficient 1 to Coefficient 64	RW

Table 6-9. Physical Pseudo Port 1 Parameter Register 0

Bit Location	Register Description	Attributes
23:22	Reserved	RO
29:24	16G Pre-Cursor Coefficient Pseudo port 1 Coefficient 1 to Coefficient 64	RW
31:30	Reserved	RO

6.10 Physical Pseudo Port 1 Parameter Register 1



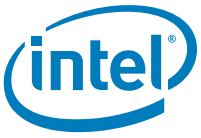


Table 6-10. Physical Pseudo Port 1 Parameter Register 1

Bit Location	Register Description	Attributes
3:0	**Downstream Pseudo Port 1, 8 GT/s TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
7:4	**Downstream Pseudo Port 1 8GT Requested TX Preset** 0000: P0 0001: P1 0010: P2 0011: P3 0100: P4 0101: P5 0110: P6 0111: P7 (Def) 1000: P8 1001: P9 1010: P10 1011 to 1111: Rsvd	RW
13:8	8G Post-Cursor Coefficient Pseudo port 1 Coefficient 1 to Coefficient 64	RW
15:14	Reserved	RO
21:16	8G Cursor Coefficient Pseudo port 1 Coefficient 1 to Coefficient 64	RW
23:22	Reserved	R0
29:24	8G Pre-Cursor Coefficient Pseudo port 1 Coefficient 1 to Coefficient 64	RW
31:30	Reserved	R0

6.11 Physical Pseudo Port 1 Parameter Register 2

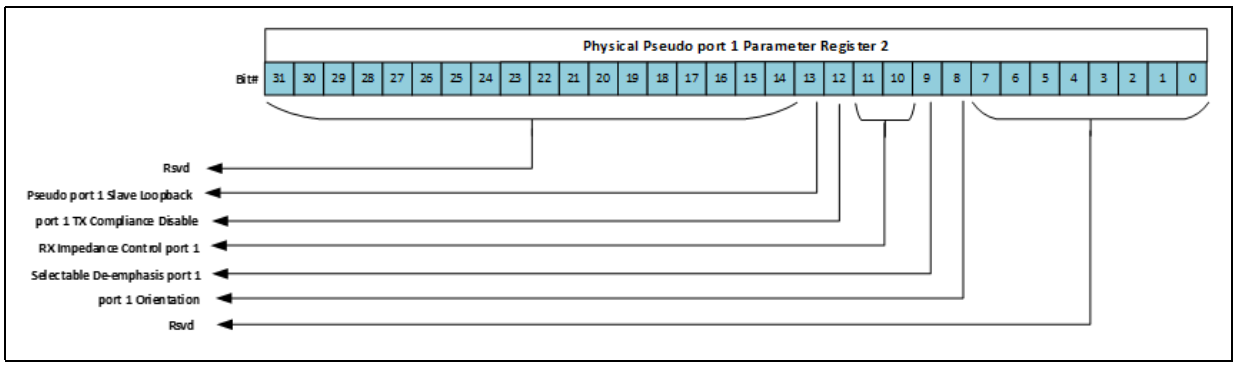
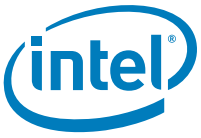


Table 6-11. Physical Pseudo Port 1 Parameter Register 2

Bit Location	Register Description	Attributes
7:0	Reserved	RO
8	**Port 1 Orientation** (valid when Port Orientation Method in Global Parameter Register = 0) 0 = Upstream (Def) 1 = Downstream	RO
9	**Selectable De-emphasis Port 0** (Valid when Port 0 orientation =1 and Link Data Rate =5G) 0 = -3.5 dB (Def) 1 = -6.0 dB	RW
11:10	**RX Impedance Control Port 1** 00: Static- On 01: Static- Off 10: Dynamic (Def) 11: Rsvd	RO
12	**Port 1 TX Compliance Disable** 1 = Disable 0 = Enable (Def)	RW
13	**Pseudo Port 1 Slave Loopback** 1 = Enable 0 = Disable (Def)	RW
31:14	Reserved	RO



6.12 Register Offsets for Different Link Subdivision (Bifurcation)

The following table shows the offsets for various registers.

Table 6-12. Register Offsets

	Offset
Global Parameter Register 0	0x0000
Global Parameter register 0	0x0004
Rsvd	0x0008
Rsvd	0x000C
Physical Pseudo Port 0 Parameter register 2	0x0010
Physical Pseudo Port 0 Parameter Register 0 Lane 0	0x0014
Physical Pseudo Port 0 Parameter register 1 Lane 0	0x0018
Physical Pseudo Port 0 Parameter register 0 Lane 1	0x001C
Physical Pseudo Port 0 Parameter register 1 Lane 1	0x0020
Physical Pseudo Port 0 Parameter register 0 Lane 2	0x0024
Physical Pseudo Port 0 Parameter register 1 Lane 2	0x0028
Physical Pseudo Port 0 Parameter register 0 Lane 3	0x002C
Physical Pseudo Port 0 Parameter register 1 Lane 3	0x0030
Physical Pseudo Port 0 Parameter register 0 Lane 4	0x0034
Physical Pseudo Port 0 Parameter register 1 Lane 4	0x0038
Physical Pseudo Port 0 Parameter register 0 Lane 5	0x003C
Physical Pseudo Port 0 Parameter register 1 Lane 5	0x0040
Physical Pseudo Port 0 Parameter register 0 Lane 6	0x0044
Physical Pseudo Port 0 Parameter register 1 Lane 6	0x0048
Physical Pseudo Port 0 Parameter register 0 Lane 7	0x004C
Physical Pseudo Port 0 Parameter register 1 Lane 7	0x0050
Physical Pseudo Port 0 Parameter register 0 Lane 8	0x0054
Physical Pseudo Port 0 Parameter register 1 Lane 8	0x0058
Physical Pseudo Port 0 Parameter register 0 Lane 9	0x005C
Physical Pseudo Port 0 Parameter register 1 Lane 9	0x0060
Physical Pseudo Port 0 Parameter register 0 Lane 10	0x0064
Physical Pseudo Port 0 Parameter register 1 Lane 10	0x0068
Physical Pseudo Port 0 Parameter register 0 Lane 11	0x006C
Physical Pseudo Port 0 Parameter register 1 Lane 11	0x0070
Physical Pseudo Port 0 Parameter register 0 Lane 12	0x0074
Physical Pseudo Port 0 Parameter register 1 Lane 12	0x0078
Physical Pseudo Port 0 Parameter register 0 Lane 13	0x007C
Physical Pseudo Port 0 Parameter register 1 Lane 13	0x0080
Physical Pseudo Port 0 Parameter register 0 Lane 14	0x0084
Physical Pseudo Port 0 Parameter register 1 Lane 14	0x0088
Physical Pseudo Port 0 Parameter register 0 Lane 15	0x008C
Physical Pseudo Port 0 Parameter register 1 Lane 15	0x0090
Rsvd	0x0094
Rsvd	0x0098
Rsvd	0x009C
Rsvd	0x00A0
Rsvd	0x00A4
Rsvd	0x00A8

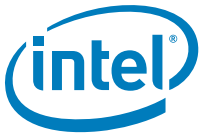


Table 6-12. Register Offsets

Physical Pseudo Port 1 Parameter register 2	0x00AC
Physical Pseudo Port 1 Parameter register 0 Lane 0	0x00B0
Physical Pseudo Port 1 Parameter register 1 Lane 0	0x00B4
Physical Pseudo port 1 Parameter register 0 Lane 1	0x00B8
Physical Pseudo port 1 Parameter register 1 Lane 1	0x00BC
Physical Pseudo port 1 Parameter register 0 Lane 2	0x00C0
Physical Pseudo port 1 Parameter register 1 Lane 2	0x00C4
Physical Pseudo port 1 Parameter register 0 Lane 3	0x00C8
Physical Pseudo port 1 Parameter register 1 Lane 3	0x00CC
Physical Pseudo port 1 Parameter register 0 Lane 4	0x00D0
Physical Pseudo port 1 Parameter register 1 Lane 4	0x00D4
Physical Pseudo port 1 Parameter register 0 Lane 5	0x00D8
Physical Pseudo port 1 Parameter register 1 Lane 5	0x00DC
Physical Pseudo port 1 Parameter register 0 Lane 6	0x00E0
Physical Pseudo port 1 Parameter register 1 Lane 6	0x00E4
Physical Pseudo port 1 Parameter register 0 Lane 7	0x00E8
Physical Pseudo port 1 Parameter register 1 Lane 7	0x00EC
Physical Pseudo port 1 Parameter register 0 Lane 8	0x00F0
Physical Pseudo port 1 Parameter register 1 Lane 8	0x00F4
Physical Pseudo port 1 Parameter register 0 Lane 9	0x00F8
Physical Pseudo port 1 Parameter register 1 Lane 9	0x00FC
Physical Pseudo port 1 Parameter register 0 Lane 10	0x00100
Physical Pseudo port 1 Parameter register 1 Lane 10	0x0104
Physical Pseudo port 1 Parameter register 0 Lane 11	0x0108
Physical Pseudo port 1 Parameter register 1 Lane 11	0x010C
Physical Pseudo port 1 Parameter register 0 Lane 12	0x0110
Physical Pseudo port 1 Parameter register 1 Lane 12	0x0114
Physical Pseudo port 1 Parameter register 0 Lane 13	0x0118
Physical Pseudo port 1 Parameter register 1 Lane 13	0x011C
Physical Pseudo port 1 Parameter register 0 Lane 14	0x0120
Physical Pseudo port 1 Parameter register 1 Lane 14	0x0124
Physical Pseudo port 1 Parameter register 0 Lane 15	0x0128
Physical Pseudo port 1 Parameter register 1 Lane 15	0x012C
Rsvd	0x0130
Rsvd	0x0134
Rsvd	0x0138
Rsvd	0x013C
Rsvd	0x0140
Rsvd	0x0144
Rsvd	0x0148
Rsvd	0x014C
Rsvd	0x0150
Rsvd	0x0154
Rsvd	0x0158
Rsvd	0x015C
Rsvd	0x0160
Rsvd	0x0164
Vendor Defined	0x0168

Offsets from 0x0168 onwards can be used for vendor defined purposes.

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